

AM64x/AM243x GENERAL PURPOSE EVM BOARD
PROC101A

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REV	A
VER	0.6



REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	10th FEBRUARY 2021	Drafted from "PROC101E2_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th FEBRUARY 2021	1.C400,C441 changed from 0402 to 0603 2.LD26 changed from red to green is followed as mentioned in the data manual 3.Capacitor Divider with value 27pF is introduced at the XI input of U15 (CPSW Ethernet PHY) as the source/driver is 3.3V and XI input accepts an input of 1.5V to 1.9V P-P. 4.MUX IC U78 is removed and the CPSW_RGMII1_MDIO/MDC pins are directly connected to SoC pins P5 & R2 Respectively. 5.R370 is mounted with 1.5K resistor 6.R183 made DNI as the desired input to the inverter U47 should be high 7.R605,a pull-down resistor of value 499E 1% is added on the USB0_RCALIB as per the recommendation in the SoC datasheet 8. 4.7K Pull up resistors are added to the 4 UART TX pins (R608,R609,R610,R611) 9.R606,a 4.7K Pull down resistor is added at pin MCU_PORz to Ensure that the MCU_PORz is low at the start of the power down sequence 10.R348 changed from 1K to 10K 11.DC Jack changed from PJ-063AH to PJ-080BH 12.J21 changed from 7499151120 to LP1G17512AONL 13.Q20,Q21,R612, R613, R614, R615, R616, R617 added for status leds of ethernet phys 14.R313,R316 removed 15.Display changed to OSD9616P1673-30	Mistral Design Team	AJIT MB	AJIT MB
0.3	18th FEBRUARY 2021	1.R622,R623-1K pull down resistors ; R624,R625-1.5K pull up resistors ; R632 added in PCIE clock section 2. U39 changed to TPS22918DBVR to reduce ramp down time of VDD_MMC1;R174 removed. 3.J39,J40-1x2 Header used in JTAG EMU0/1 signals to enable WIR mode or boundary scan manually. R630,R631, R634,R635 added as pull up and pull down resistors 4.R455,R458,R460,R461 made DNI. ACC14 ,ACC15 added. 5.FSI TX and RX signals swapped and pin9 of J7 made no connect	Mistral Design Team	AJIT MB	AJIT MB
0.4	25th FEBRUARY 2021	1.CDCI6214 added to provide reference clock to both PCIe connector and and SoC side 2.R448 changed from 10E to 100E 3.R685 100E Series Resistor added on JTAG_TRST# near cTI 20pin connector 4.C529 added in JTAG_TRST# from MIPI and CTI 20 connector 5. Added 10K PU resistor on JTAG_TCK, JTAG_TMS, and JTAG_TDI. Added 10K PD resistor on JTAG_TRST# 6.Added DNI 10K pull-up on MMC1_CLK . Added DNI 10K pull-down on MMC0_CLK and MMC1_CLK.	Mistral Design Team	AJIT MB	AJIT MB
0.5	28th FEBRUARY 2021	1.R622,R623-1K pull down resistors ; R624,R625-1.5K pull up resistors made as DNI 2. C502 / C503 changed to 0E 0402 Resistors -R679, R680 3. Added Resistors R661,R662, R665,R666,R667,R668 for PCIe CLK selection	Mistral Design Team	AJIT MB	AJIT MB
0.6	30th MARCH 2021	1.Added AM243x SoC variant 2. Changed core voltage supply to 0.85V in AM243x variant	Mistral Design Team	AJIT MB	AJIT MB

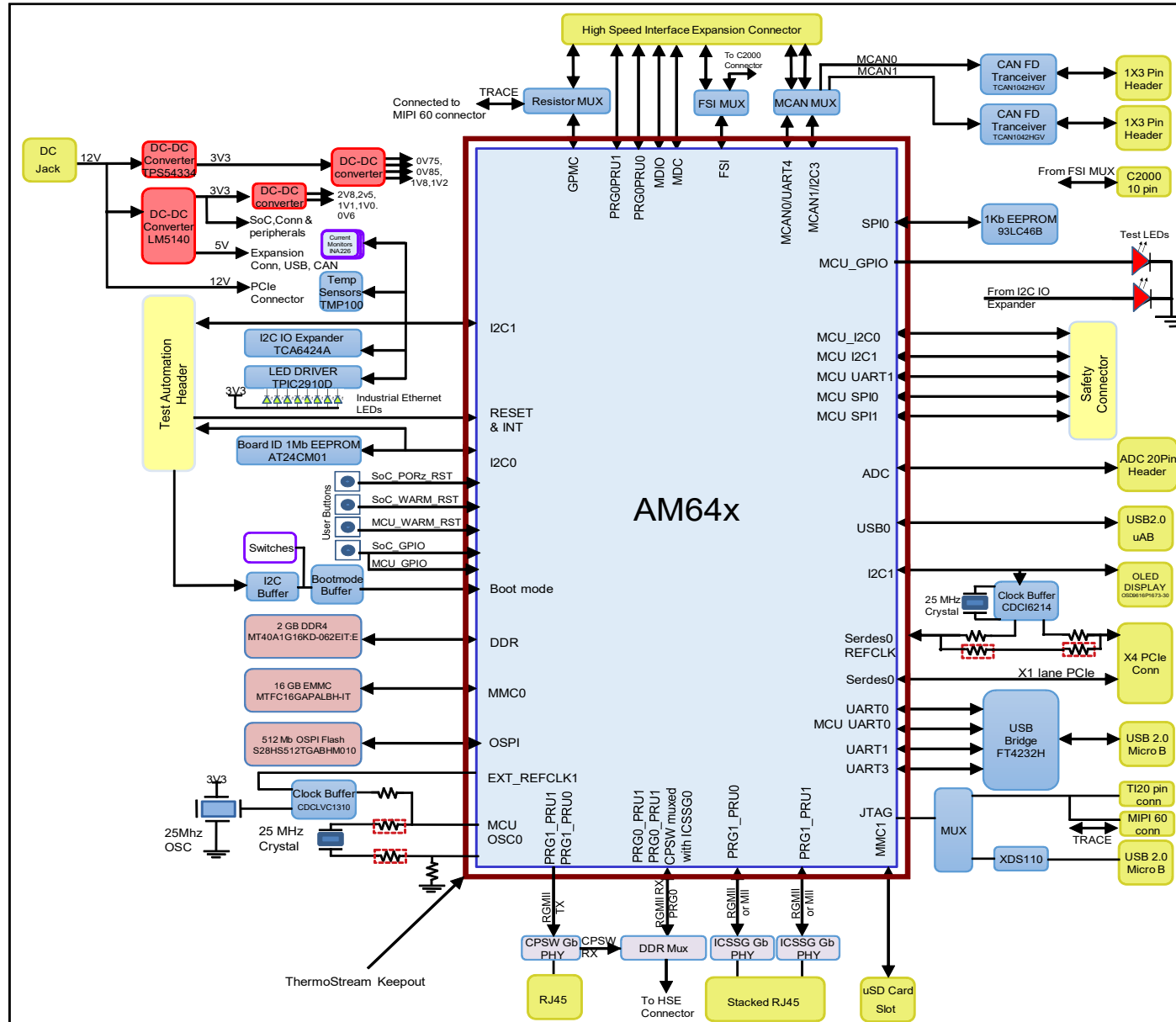
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Title REVISION HISTORY

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
C		E2
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BLOCK DIAGRAM_AM64x_EVM



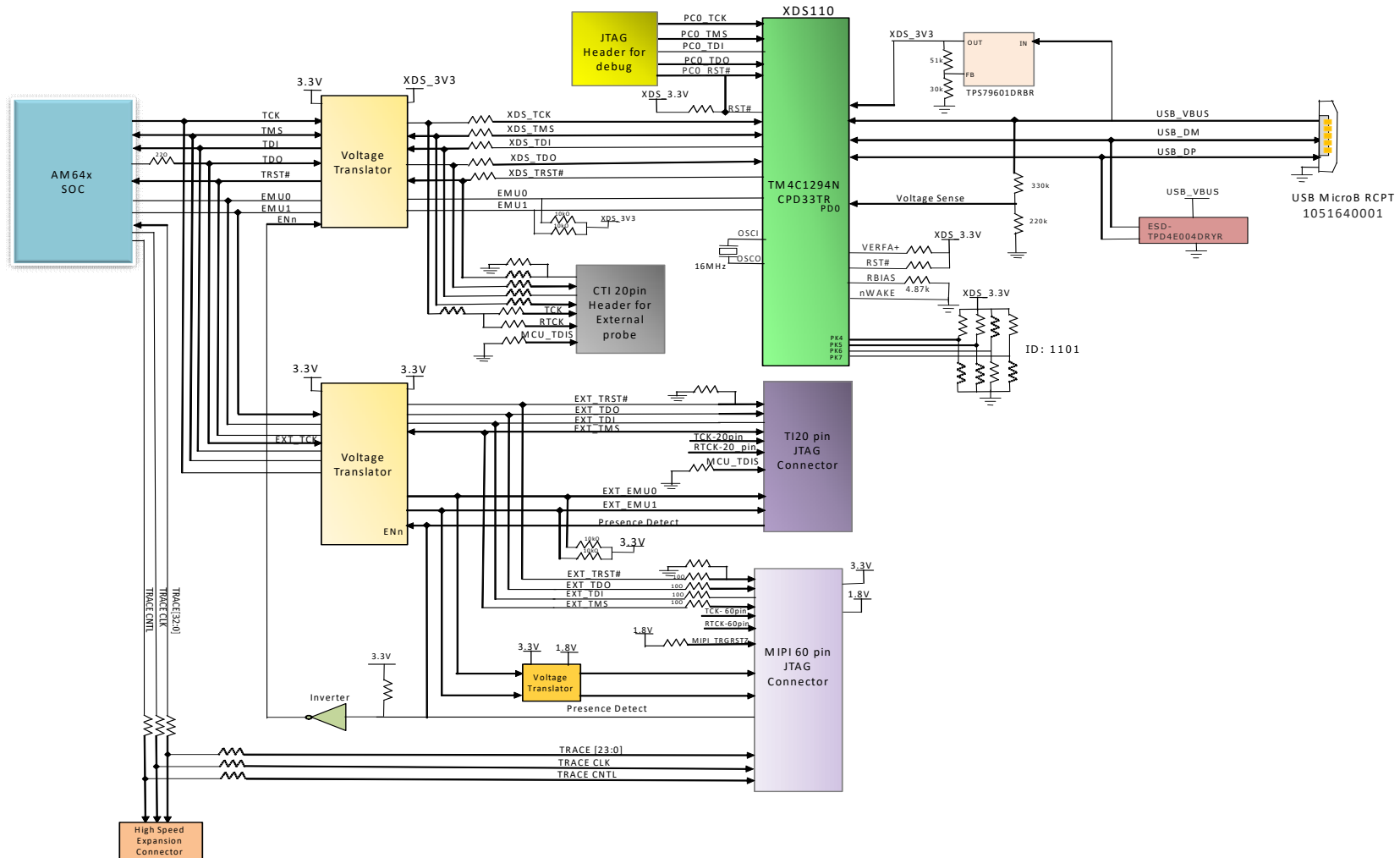
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Title BLOCK DIAGRAM_CP BOARD

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
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BLOCK DIAGRAM_XDS110



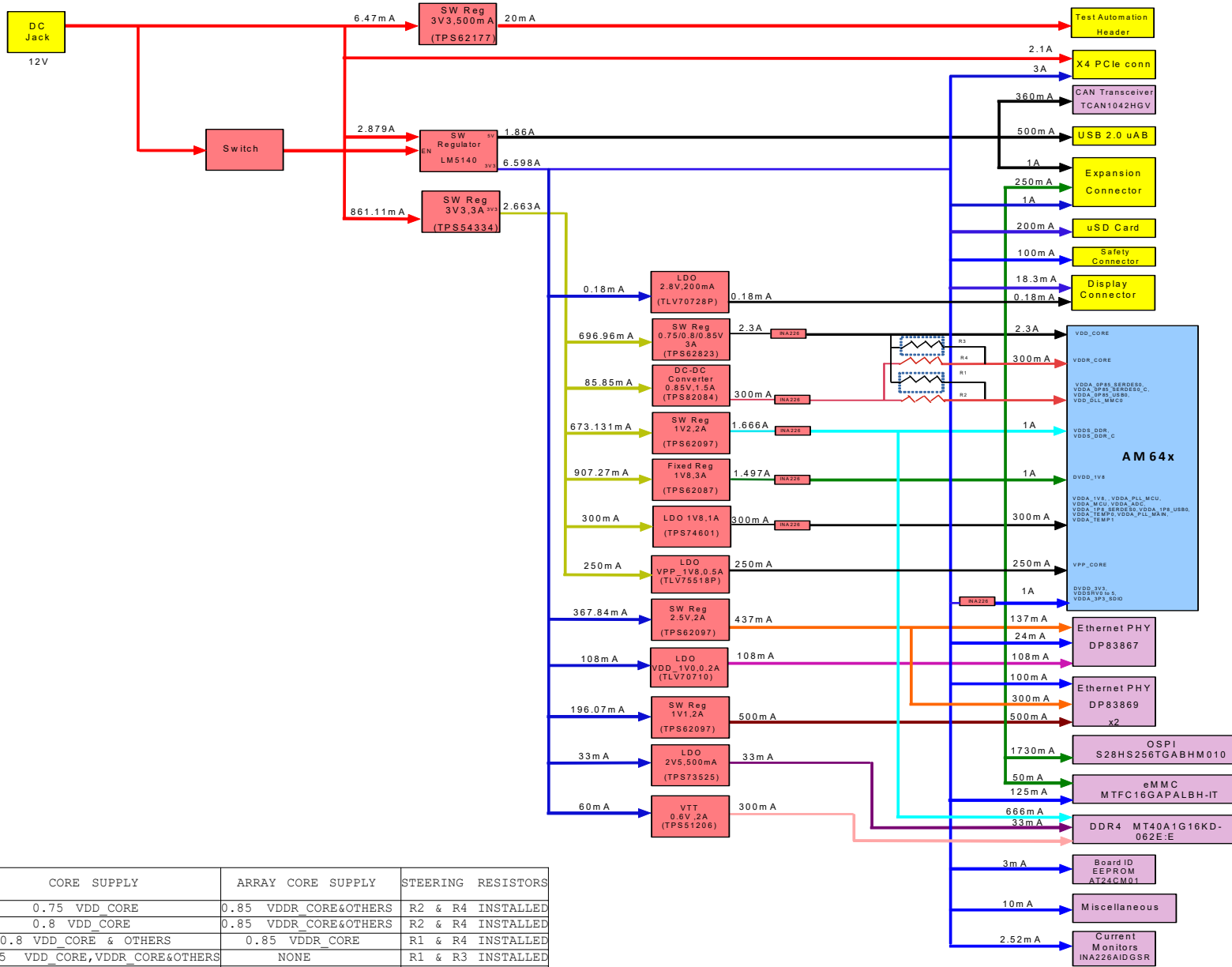
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Title BLOCK DIAGRAM_XDS110

Size	Variant Name = PROC101A(001) TMD64GPEVM	Rev
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POWER FLOW DIAGRAM



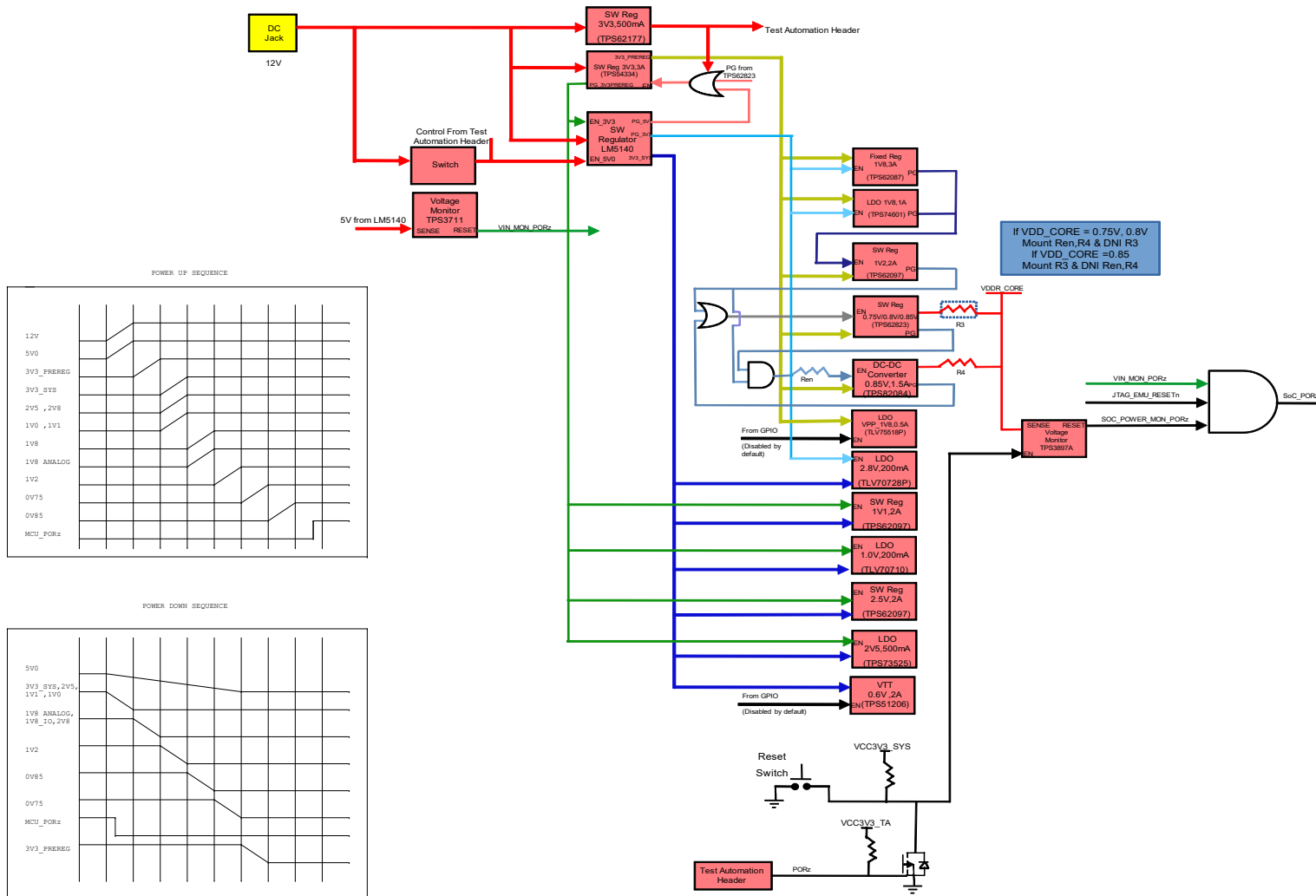
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Title POWER FLOW DIAGRAM

Size	Variant Name = PROC101A(001) TMD64GPEVM	Rev
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POWER SEQUENCE



GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETh	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

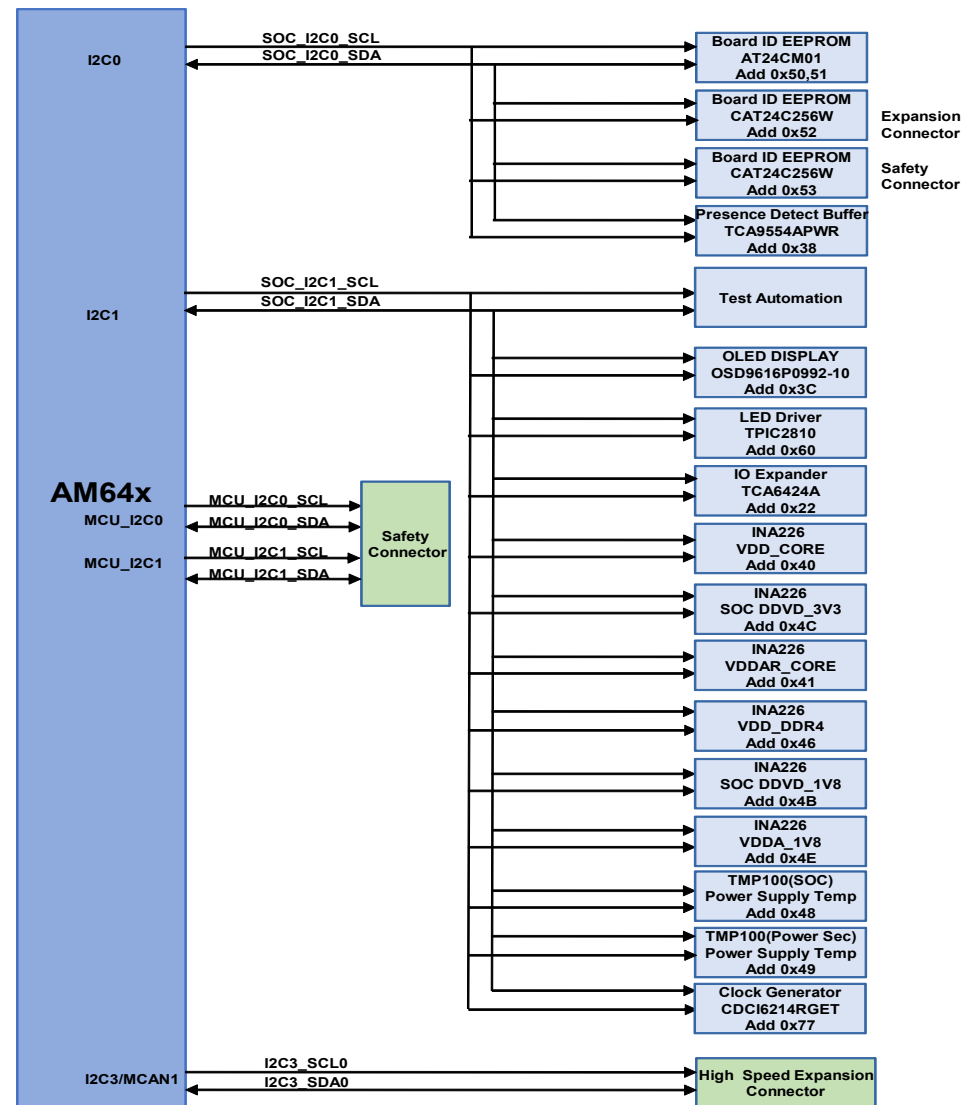
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC101A(001) TMD64GPEVM	Rev
C		E2
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I2C TREE



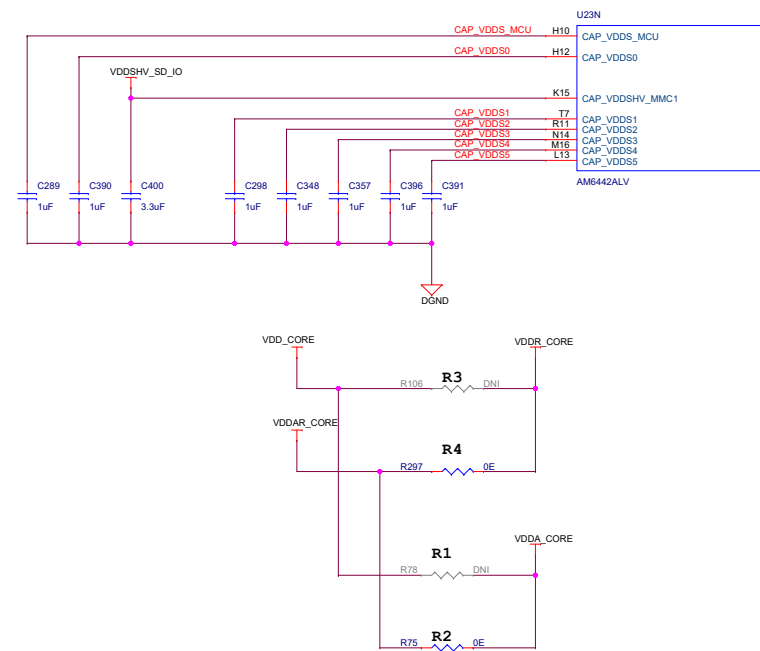
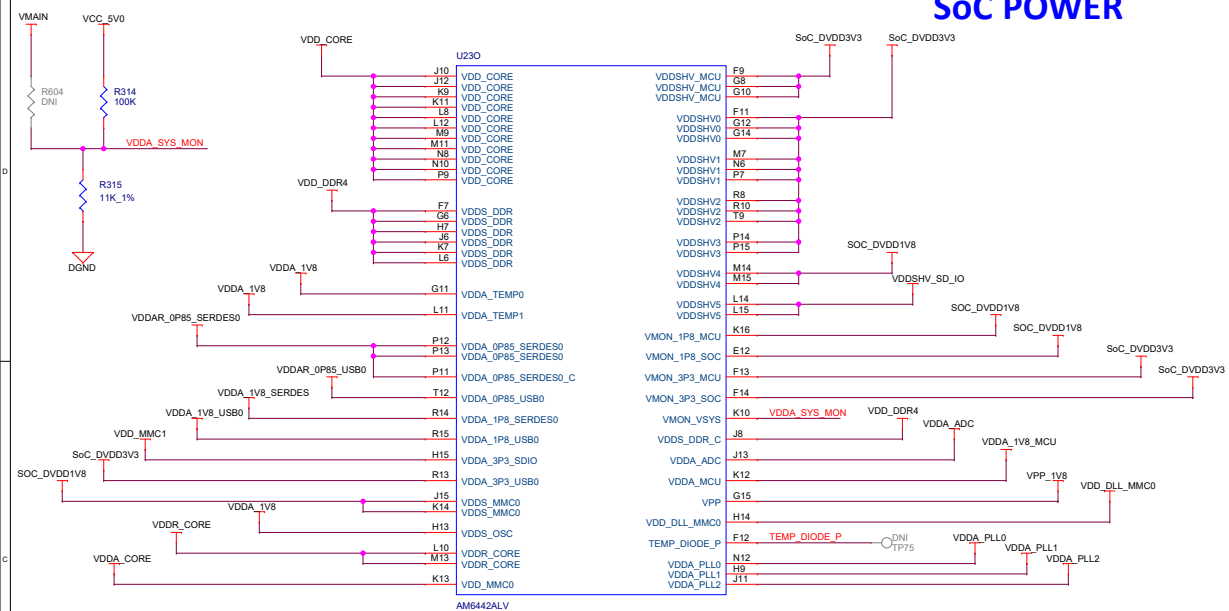
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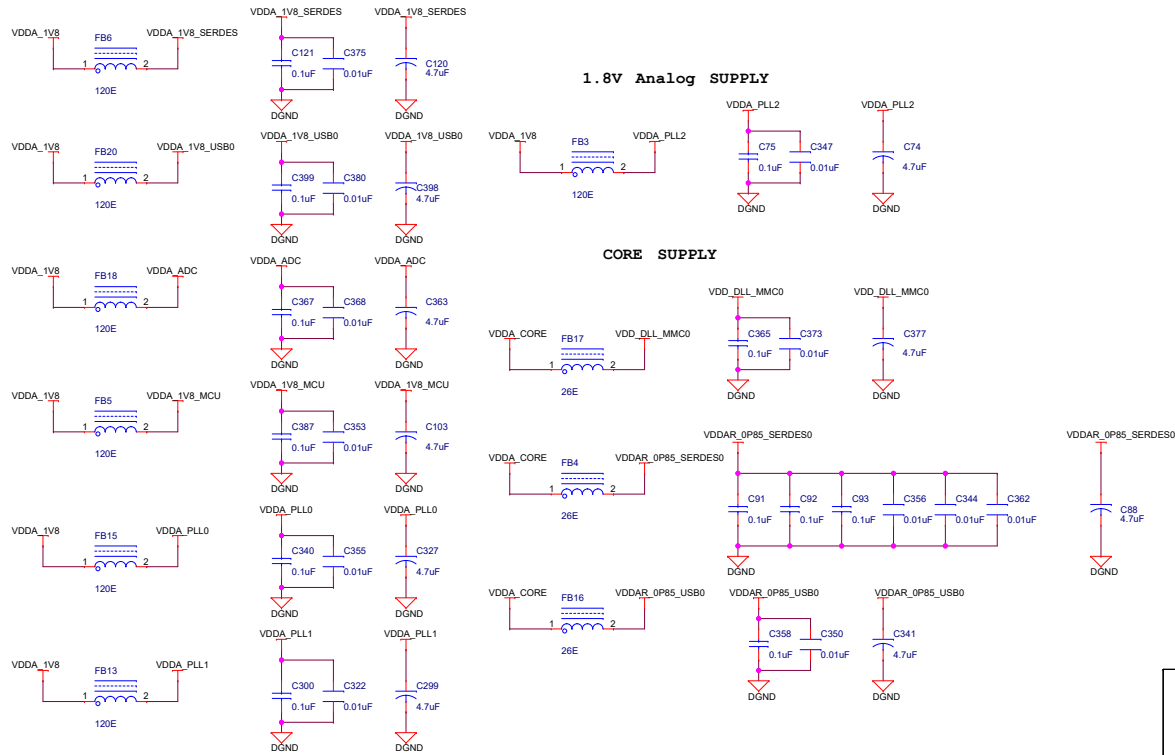
Title I2C TREE

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
C		E2
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SoC POWER

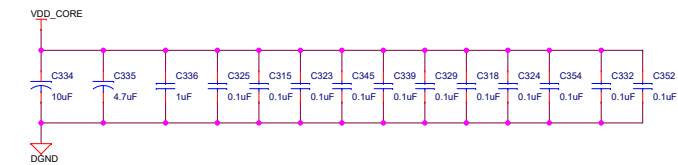


1.8V Analog SUPPLY

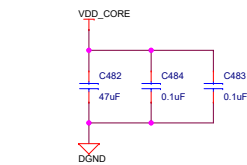


CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

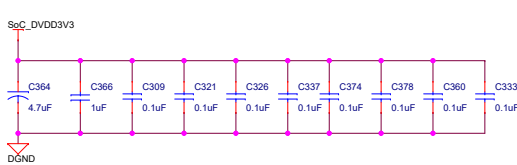
SoC POWER Decaps



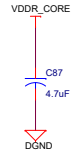
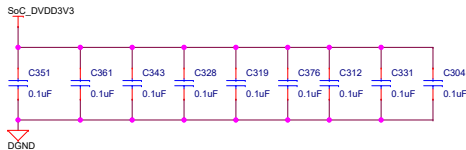
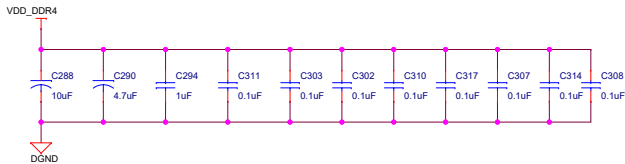
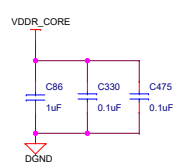
Place one 0.1uF cap near each Pin



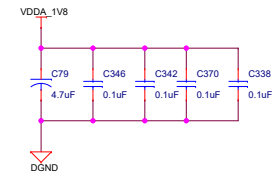
To place after current sense resitor on VDD_CORE plane



Place one 0.1uF cap near each Pin

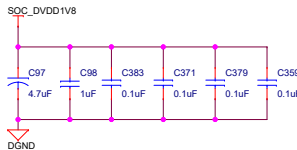
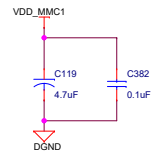


VDD ARRAY CORE

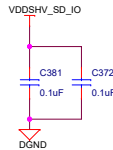


Place one 0.1uF cap near each Pin

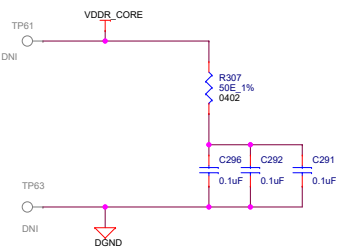
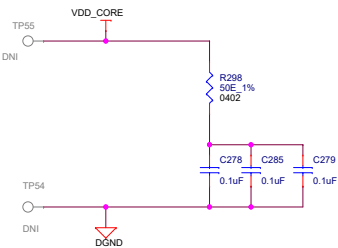
VDDA_3P3_SDIO



Place one 0.1uF cap near each Pin



Core & Array Core Supply Kelvin Sensing



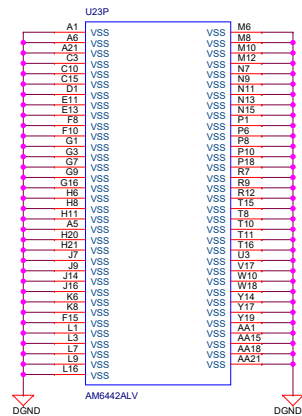
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Title SOC POWER CAPS

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
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SoC POWER - VSS



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Title SOC VSS

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C		E2
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D2G			
D2	D0R0_A0	D0R0_DM0	B2
C5	D0R0_A1	D0R0_DM1	M2
D4	D0R0_A2		A3
D3	D0R0_A3		D2
D2	D0R0_A4		D0R0_D0
J2	D0R0_A5		B5
J3	D0R0_A6		A4
J4	D0R0_A7		B3
J5	D0R0_A8		D0R0_D2
K3	D0R0_A9		C4
J4	D0R0_A10		C2
K3	D0R0_A11		D0R0_D07
M5	D0R0_A12		B4
K4	D0R0_A13		D0R0_D02
			N5
G4	D0R0_BA0		L2
G5	D0R0_BA1		D0R0_D015
			D0R0_D014
G2	D0R0_BG0		M3
H3	D0R0_BT0		D0R0_D010
K2	D0R0_ATB0		N4
K1	D0R0_ATB1		D0R0_D09
			N3
F1	D0R0_CK0		D0R0_D012
E1	D0R0_CK0_N		M4
			D0R0_D011
F4			N2
F3			D0R0_D015
E3			C1
E4			D0R0_LDQ5_P
E5			N1
F5			D0R0_LDQ5_N
H2			
H1			
H5			
J5			
K5			
F6			
D5			
H4			

TERMINATION

The diagram illustrates the termination network for a DDR3 memory module. It shows a 16-bit data bus with 16 pairs of signals (DDR_A0 to DDR_A15) connected to a 16-bit address bus (DDR_A0 to DDR_A15). The signals are terminated to VDD_DDR4 and VDD_DDR4_TTT. The termination network includes resistors R69, R63, R62, R247, R251, R267, R269, R46, R56, R73, R288, R55, R289, R90, R86, R89, R290, R77, R84, R91, R291, R83, R88, R71, R264, R271, R274, R87, and R258. The signals are also connected to a 16-bit data bus (DDR_A0 to DDR_A15) and a 16-bit address bus (DDR_A0 to DDR_A15).

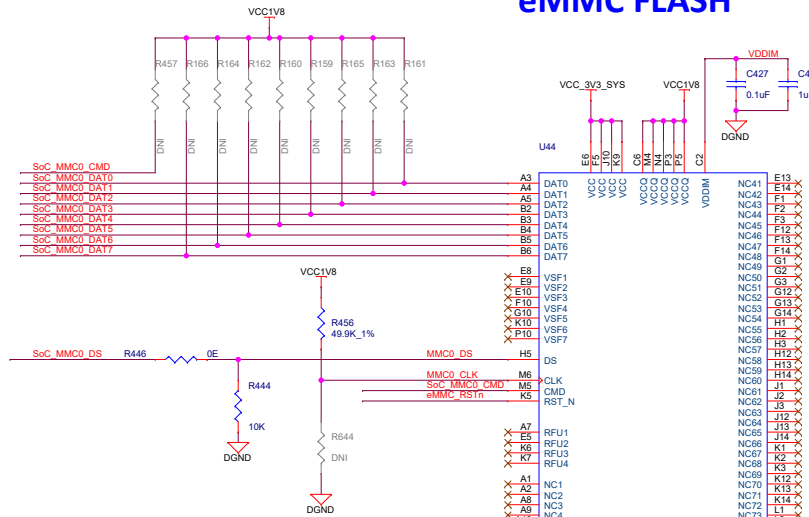
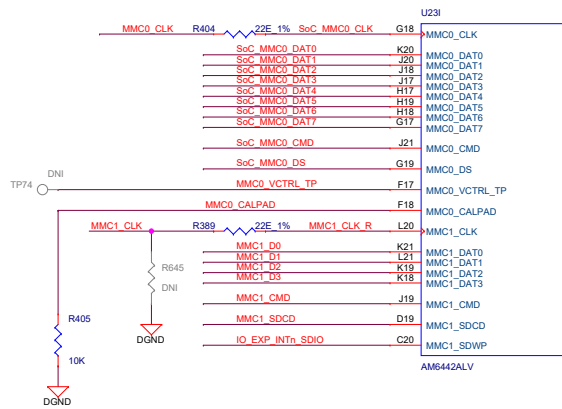


TEXAS
INSTRUMENTS

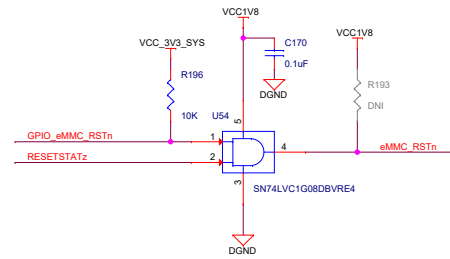


Size	Variant Name = PROC101A(001) TMDS64GPEVM	Rev
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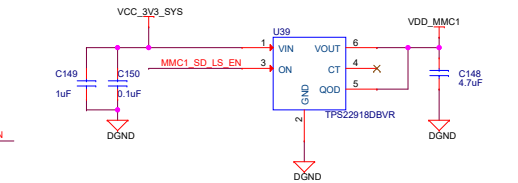
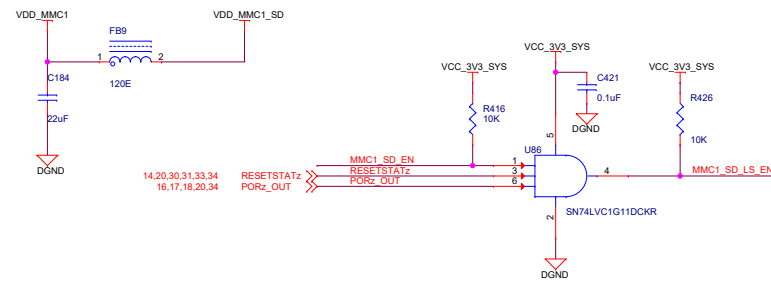
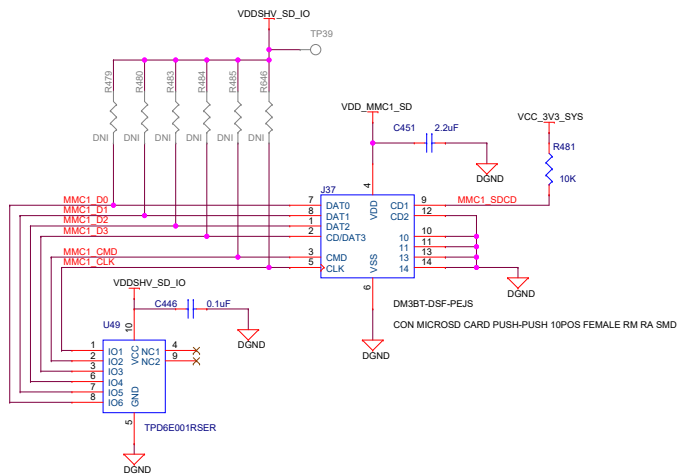
eMMC FLASH



eMMC FLASH RESET



SD CARD INTERFACE



Off Page Connections

From & To IO Expander	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

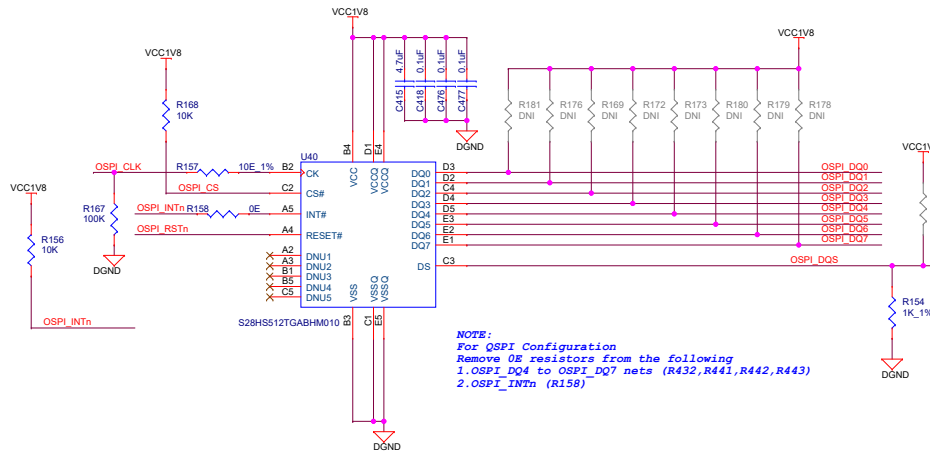
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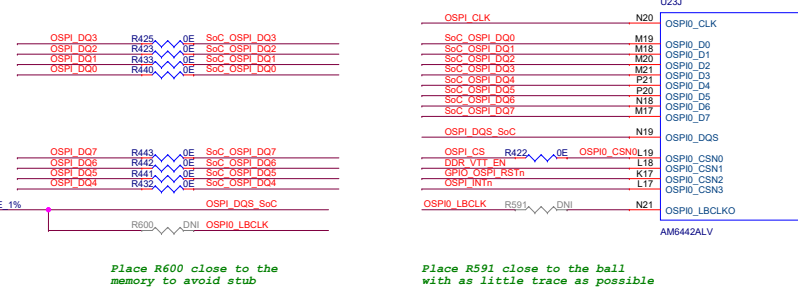
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Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
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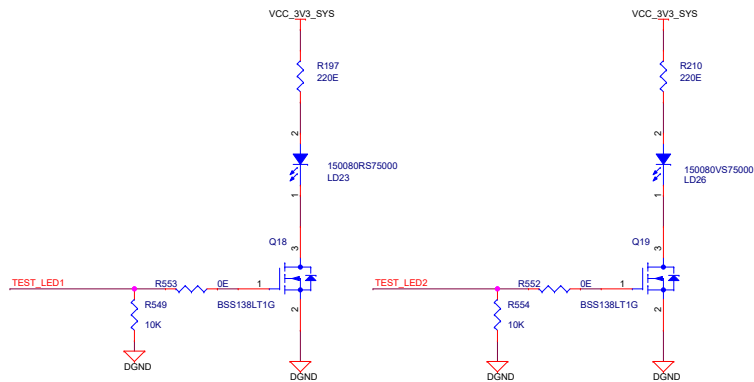
OSPI FLASH



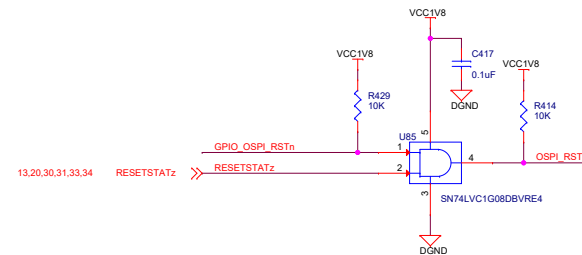
SOC OSPI INTERFACE



USER TEST LED



OSPI FLASH RESET



Off Page Connections

TEST_LED1	TEST_LED1	33
TEST_LED2	TEST_LED2	34
DDR_VTT_EN	DDR_VTT_EN	33

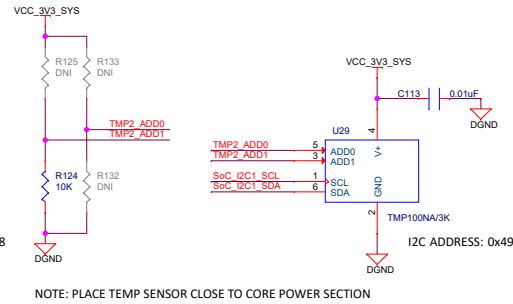
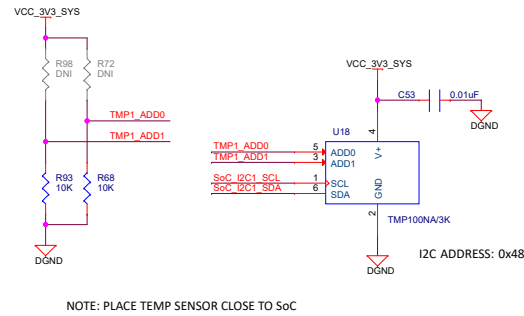
To Level Translator

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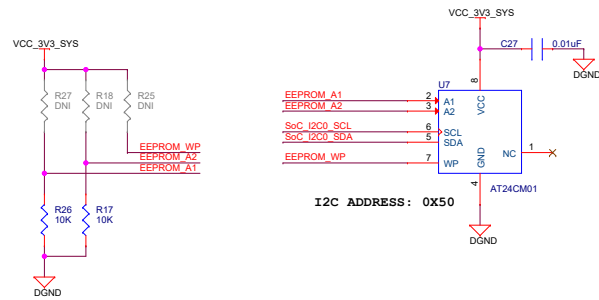
Title OSPI		Rev
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TEMPERATURE SENSOR

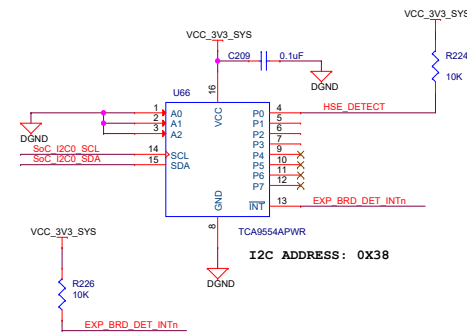


SoC_I2C1_SCL DNI TP25
SoC_I2C1_SDA DNI TP27

BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

HSE_DETECT	←	HSE_DETECT	27
SoC_I2C1_SDA	↔	SoC_I2C1_SDA	19,21,29,30,31,32,33
SoC_I2C1_SCL	↔	SoC_I2C1_SCL	19,21,29,30,31,32,33
SoC_I2C0_SDA	↔	SoC_I2C0_SDA	27,29,33
SoC_I2C0_SCL	↔	SoC_I2C0_SCL	27,29,33

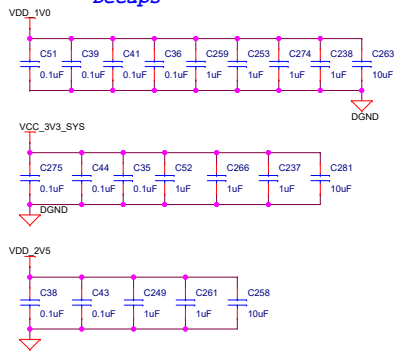
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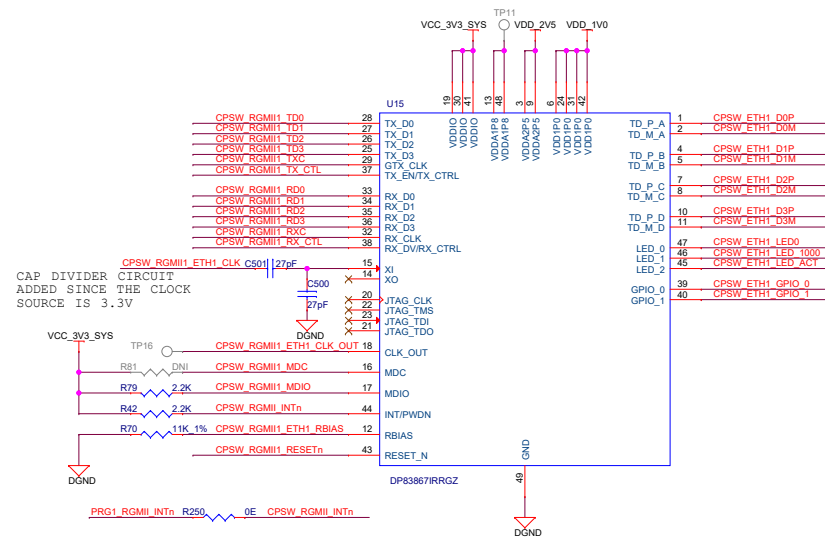
Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 15 of 40

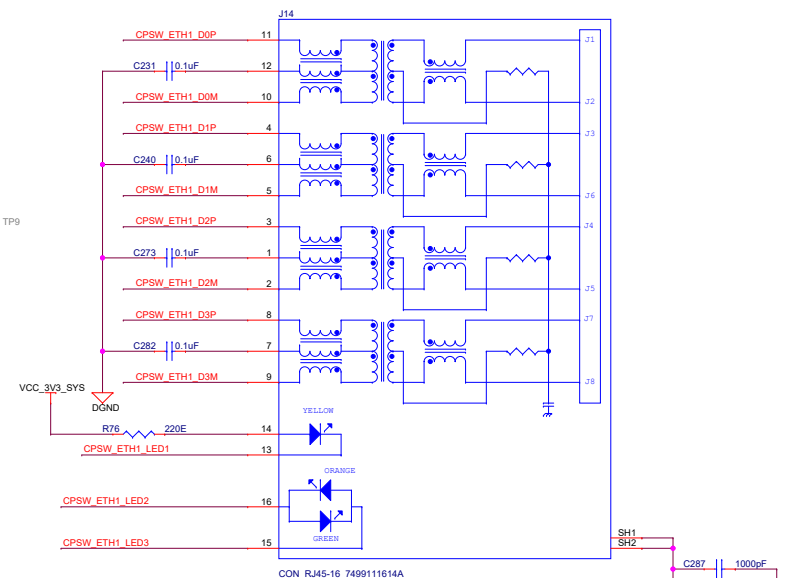
Decaps



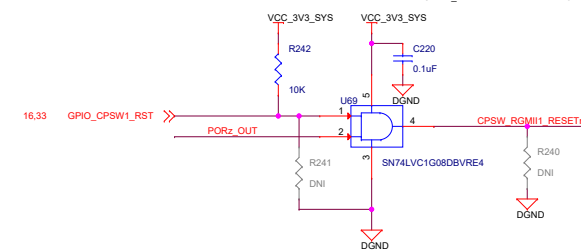
CPSW RGMII 1 - PHY



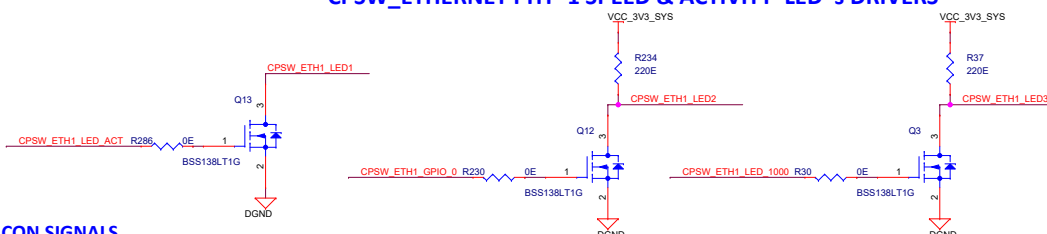
RJ45 with Integrated Magnetics



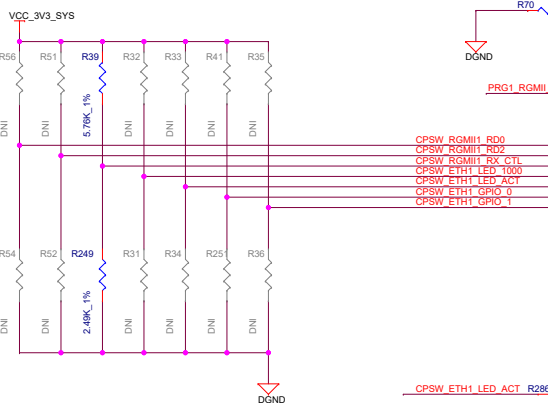
CPSW ETH1 RESET



CPSW_ETHERNET PHY-1 SPEED & ACTIVITY LED's DRIVERS

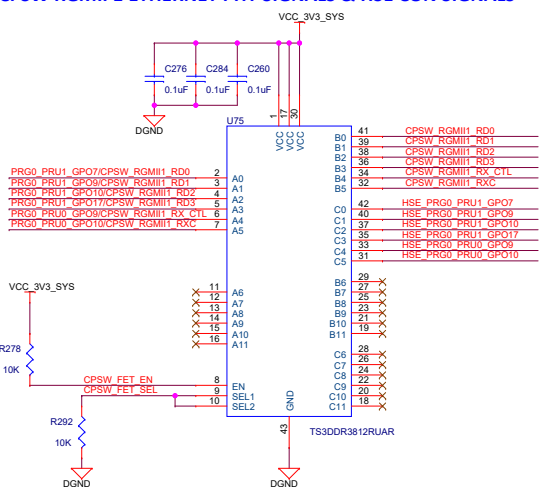


STRAPPING RESISTORS



PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns

CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

Off Page Connections

From Processor	27	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0
	27	PRG0_PRU1_GPO8/CPSW_RGMII1_RD1	PRG0_PRU1_GPO8/CPSW_RGMII1_RD1
	27	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2
	27	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3
	27	PRG0_PRU0_GPO0/CPSW_RGMII1_RX_CTL	PRG0_PRU0_GPO0/CPSW_RGMII1_RX_CTL
	27	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC
From Processor	27	CPSW_RGMII1_TD0	CPSW_RGMII1_TD0
	27	CPSW_RGMII1_TD1	CPSW_RGMII1_TD1
	27	CPSW_RGMII1_TD2	CPSW_RGMII1_TD2
	27	CPSW_RGMII1_TD3	CPSW_RGMII1_TD3
	27	CPSW_RGMII1_TX_CTL	CPSW_RGMII1_TX_CTL
	27	CPSW_RGMII1_TXC	CPSW_RGMII1_TXC
	13,17,18,20,34	PORz_OUT	PORz_OUT
	17,18,34	PRG1_RGMII1_INTn	PRG1_RGMII1_INTn
From IO Expander	16,33	GPIO_CPSW1_RST	GPIO_CPSW1_RST
	33	CPSW_FET_SEL	CPSW_FET_SEL
From Clock Buffer	31	CPSW_RGMII1_ETH1_CLK	CPSW_RGMII1_ETH1_CLK
To HSE Connector	27	HSE_PRG0_PRU1_GPO7	HSE_PRG0_PRU1_GPO7
	27	HSE_PRG0_PRU1_GPO9	HSE_PRG0_PRU1_GPO9
	27	HSE_PRG0_PRU1_GPO10	HSE_PRG0_PRU1_GPO10
	27	HSE_PRG0_PRU1_GPO17	HSE_PRG0_PRU1_GPO17
	27	HSE_PRG0_PRU0_GPO9	HSE_PRG0_PRU0_GPO9
	27	HSE_PRG0_PRU0_GPO10	HSE_PRG0_PRU0_GPO10
From Processor	17,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	17,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC

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Title CPSW RGMII1 ETHERNET PHY

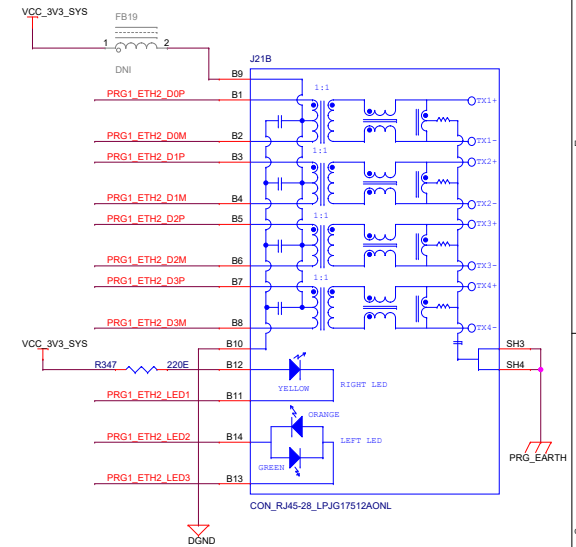
Size Variant Name = PROC101A(001) TMS64GPEVM

Date: Friday, March 26, 2021

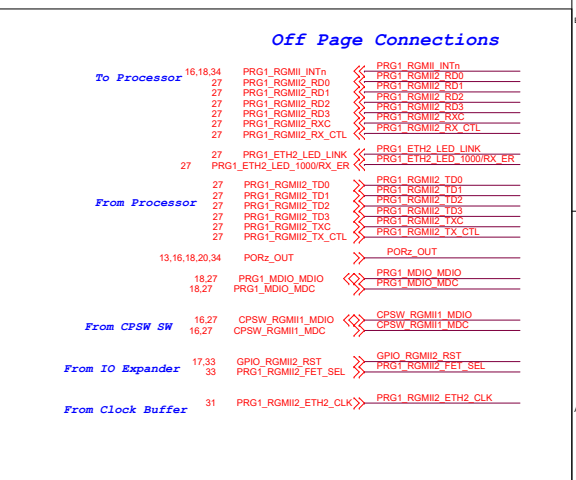
Rev E2

Sheet 16 of 40

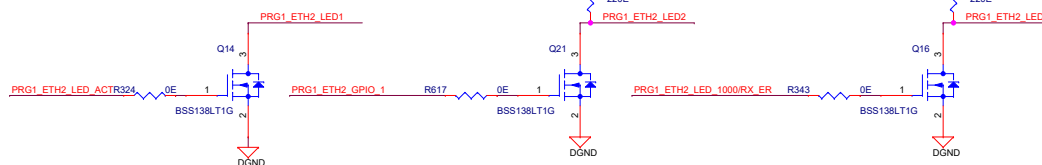
Dual RJ45 CON With Integrated Magnetics



PRG1_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



PRG1_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



Off Page Connections

To Processor	16,18,34	PRG1_RGMII_IN0	PRG1_RGMII_INn
	27	PRG1_RGMII_RD0	PRG1_RGMII_RDn
	27	PRG1_RGMII_RD1	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD2	PRG1_RGMII_RD3
	27	PRG1_RGMII_RD3	PRG1_RGMII_RD4
	27	PRG1_RGMII_RX_CTL	PRG1_RGMII_RX_CTL
	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
From Processor	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000RX_ER	PRG1_ETH2_LED_1000RX_ER
	27	PRG1_RGMII_TD0	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD1	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD2	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	PRG1_RGMII_TX_CTL
	13,16,18,20,34	POR2_OUT	POR2_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW SW	16,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From I/O Expander	17,33	GPIO_RMI2_RST	GPIO_RMI2_RST
	17,33	PRGT_RGMII2_FET_SEL	PRGT_RGMII2_FET_SEL
	31	PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

SOL	EN	FUNCTION
X	H	Disabled
L	L	A = A0 B = B0
H	L	A = A1 B = B1

Title	ICSSG1 RGMII_2 ETHERNET PHY
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Size	Variant Name = PROC101A(001) TMD564GPEVM	
C		
Date:	Friday, March 26, 2021	Sheet 17 of 40

VCC_3V3_SVS

R310 2.49K 1%

R308 2.49K 1%

R101 DNI

R94 DNI

R95 DNI

R564 DNI

R114 DNI

R108 DNI

R107 DNI

R100 DNI

R96 DNI

R97 DNI

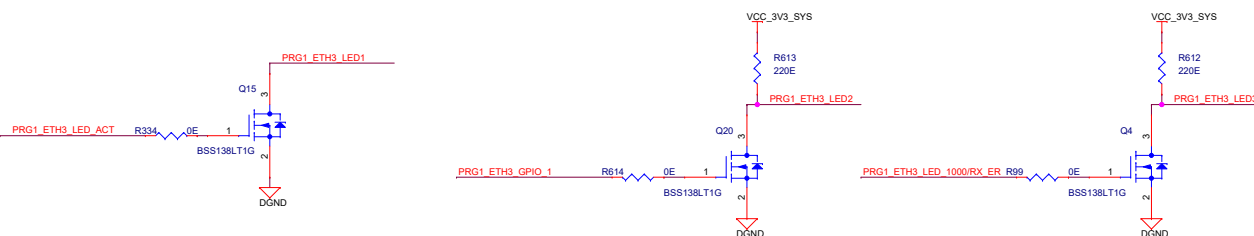
R565 2.49K 1%

R115 DNI

GND

PRG1_RGMII1_RD0
PRG1_RGMII1_RD1
PRG1_RGMII1_RX_CTL
PRG1_ETH5_LED_1000RX_ER
PRG1_ETH5_LED_ACT
PRG1_ETH5_LED_LINK
PRG1_ETH5_GPIO_1

PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



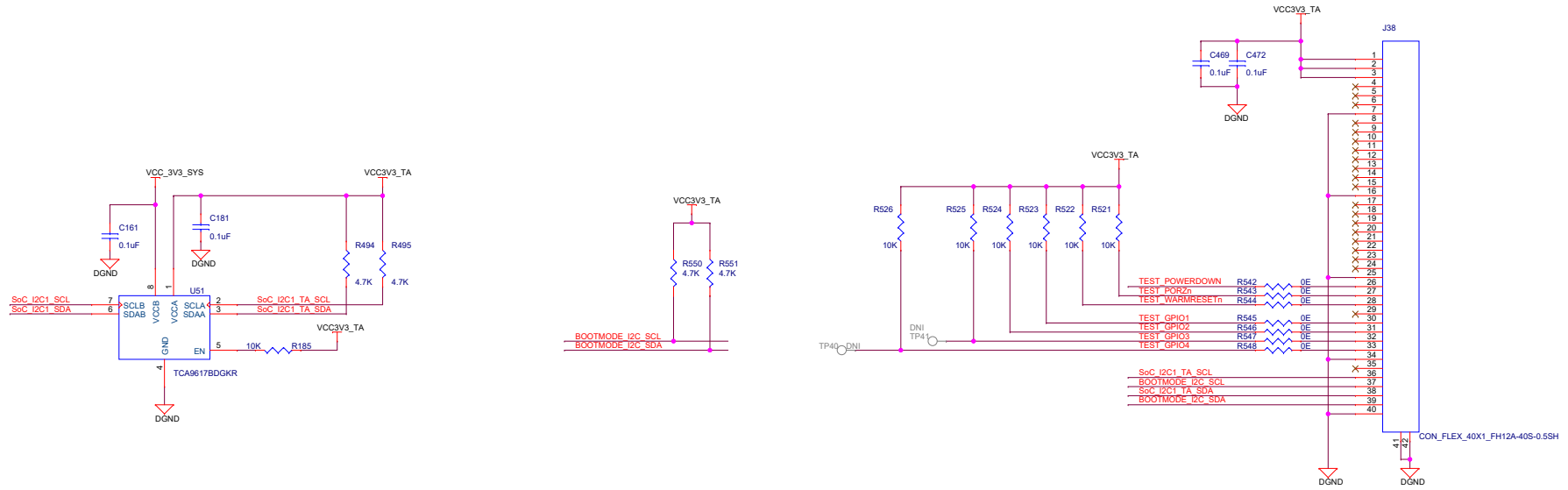
To Processor	16,17,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII_RD0	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	PRG1_RGMII_RD3
	27	PRG1_RGMII_RXC	PRG1_RGMII_RXC
	27	PRG1_RGMII_RX_CTL	PRG1_RGMII_RX_CTL
	16,16,17,20,34	PORz_OUT	PORz_OUT
From Processor	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
	27	PRG1_ETH3_LED_1000RX_ER	PRG1_ETH3_LED_1000RX_ER
	27	PRG1_RGMII_TD0	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	PRG1_RGMII_TX_CTL
From Processor	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII1_RST	GPIO_RGMII1_RST
From Clock Buffer	31	PRG1_RGMII1_ETH3_CLK	PRG1_RGMII1_ETH3_CLK



Size	Variant Name = PROC101A(001) TMSD64GPEVM	Rev
C		E2
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TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL	SoC_I2C1_SCL
	15,21,29,30,31,32,33	SoC_I2C1_SDA	SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

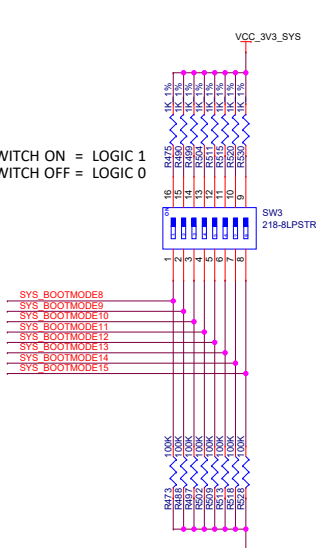
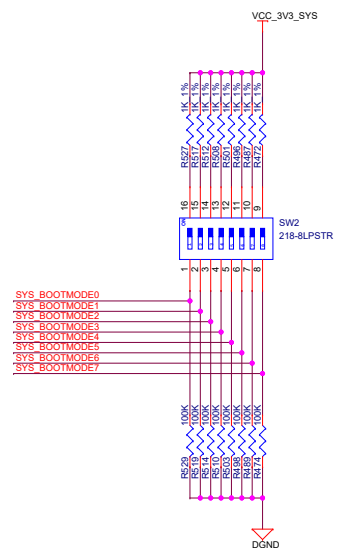
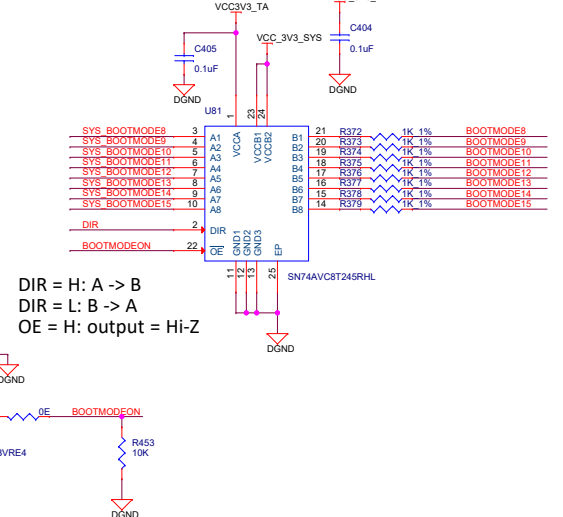
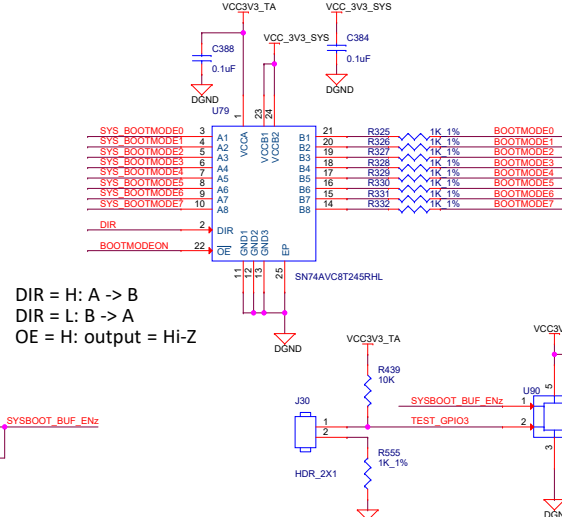
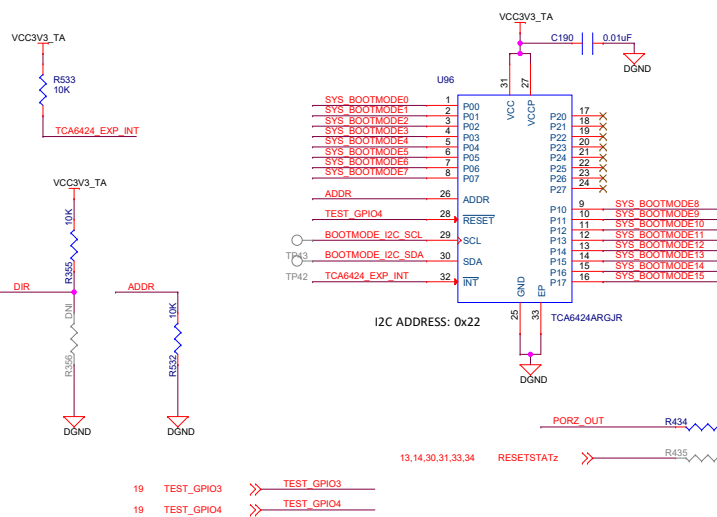
Designed for TI by Mistral Solutions Pvt Ltd



Title TEST AUTOMATION

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 19 of 40

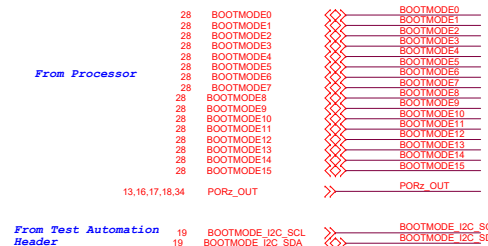
BOOT MODE BUFFER & SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections



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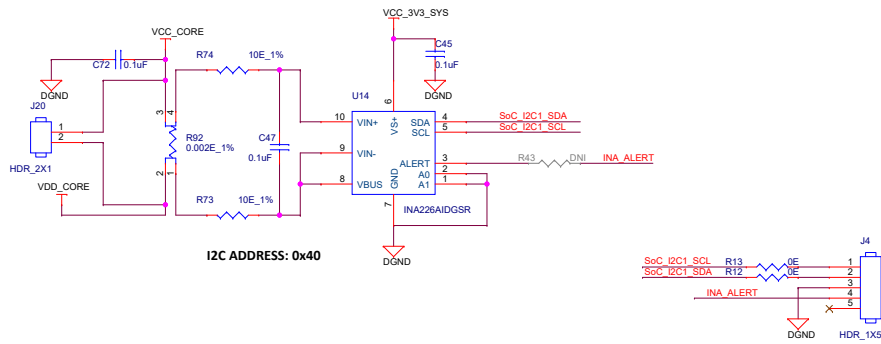


Title BOOT MODE BUFFER & SWITCHES

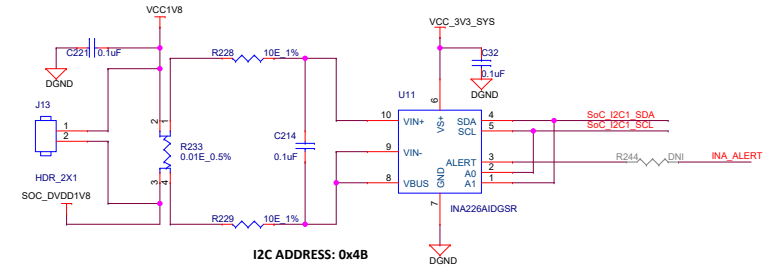
Size	Variant Name = PROC101A(001)TMD564PEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 20 of 40

CURRENT MONITORING DEVICES

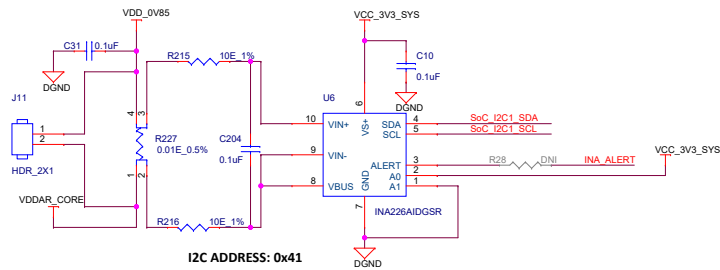
VDD_CORE



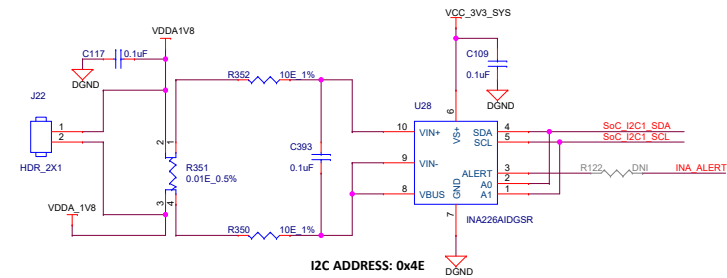
SoC_DVDD1V8



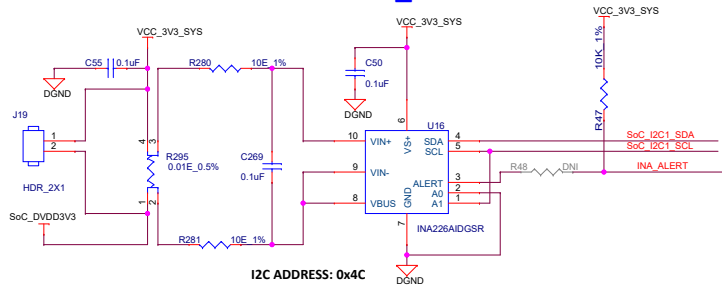
VDDAR_CORE



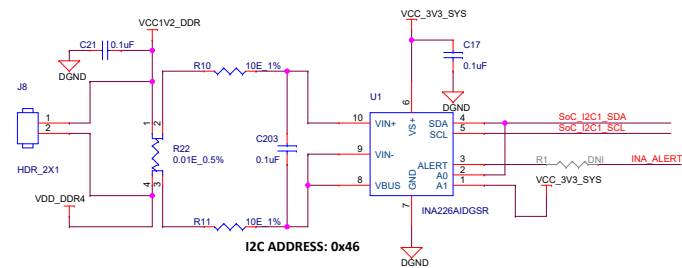
VDDA_1V8



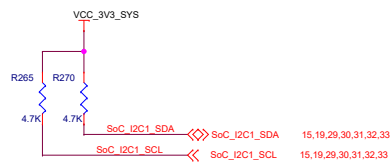
SoC_DVDD3V3



VDD_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



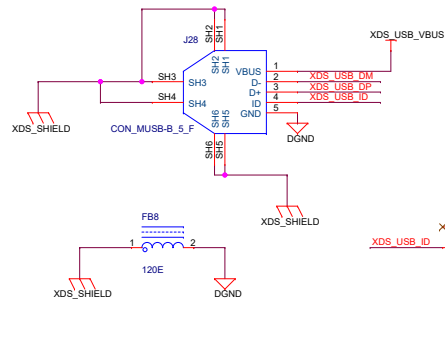
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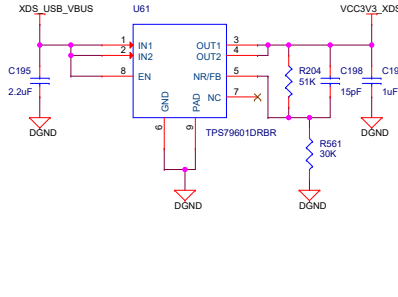
Title CURRENT MONITORING DEVICES

Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 21 of 40

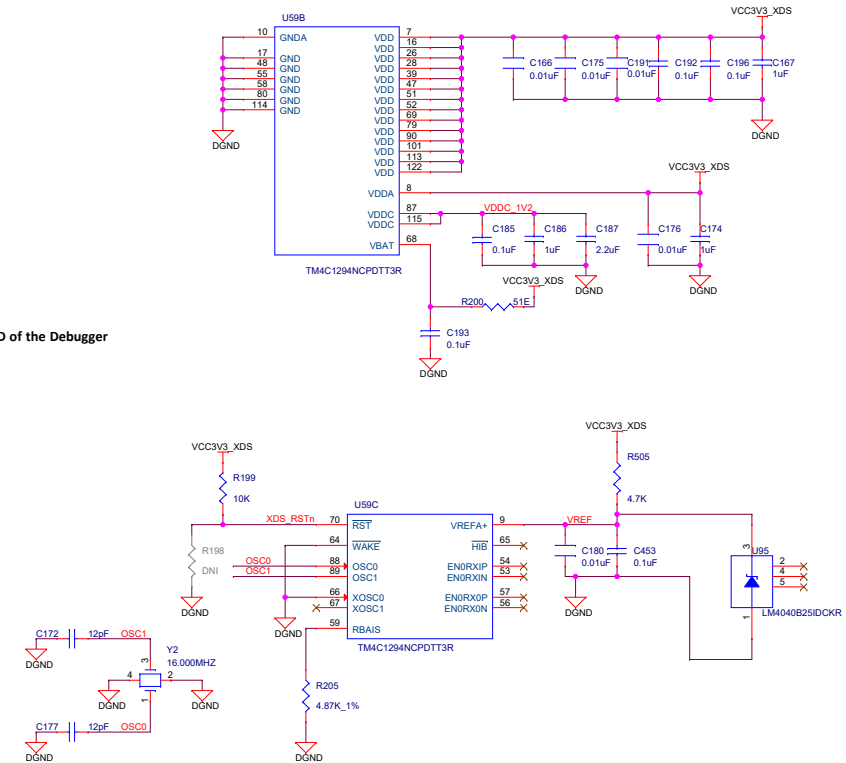
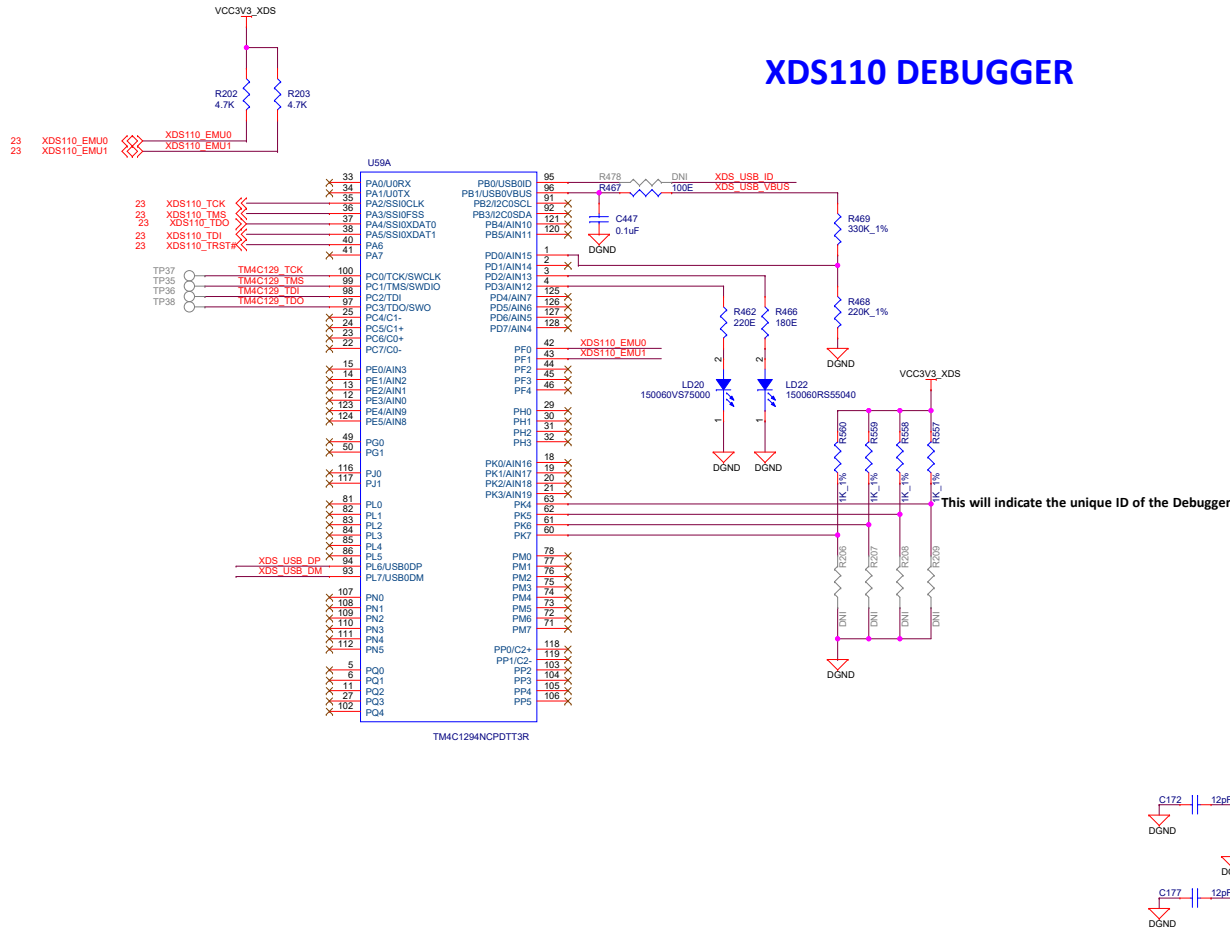
USB Connector



XDS110 POWER



XDS110 DEBUGGER



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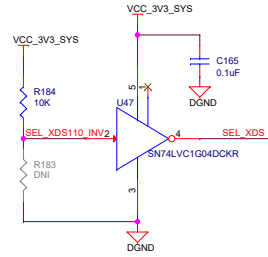
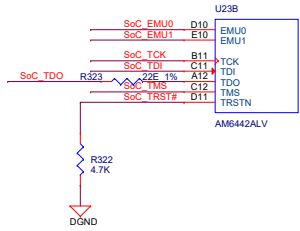


Title XDS110 DEBUGGER

Size	Variant Name = PROC101A(001) TMD64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 22 of 40

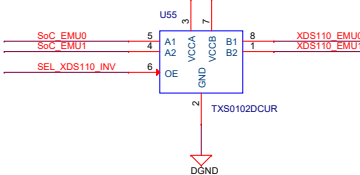
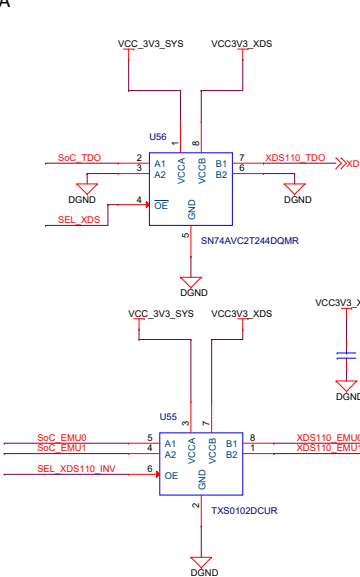
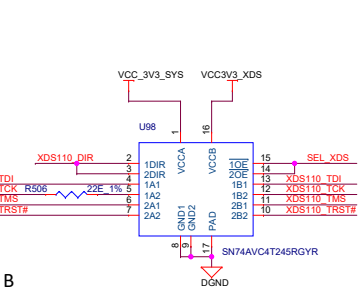
JTAG BUFFER

JTAG SoC SECTION



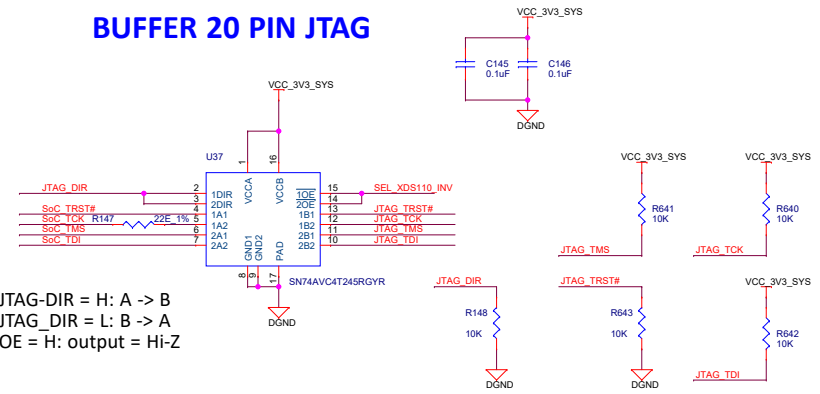
BUFFER XDS110

XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

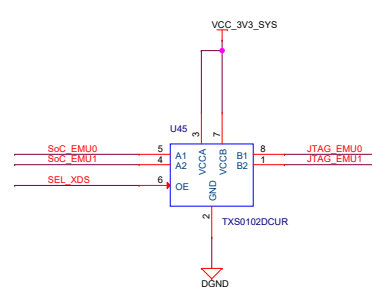
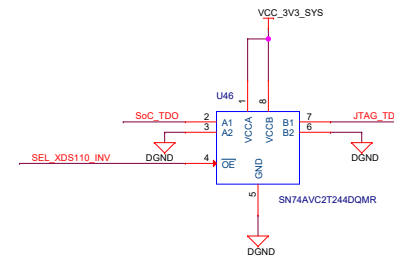


Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25

BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z



Off Page Connections

From XDS1100 Debugger

24	SEL_XDS110_INV	XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TCK
22	XDS110_TCK	XDS110_TMS
22	XDS110_TMS	XDS110_TRST#
22	XDS110_TRST#	JTAG_TCK
24	JTAG_TCK	JTAG_TMS
24	JTAG_TMS	JTAG_TRST#
24	JTAG_TRST#	JTAG_TDO
24	JTAG_TDO	XDS110_EMU0
22	XDS110_EMU0	XDS110_EMU1

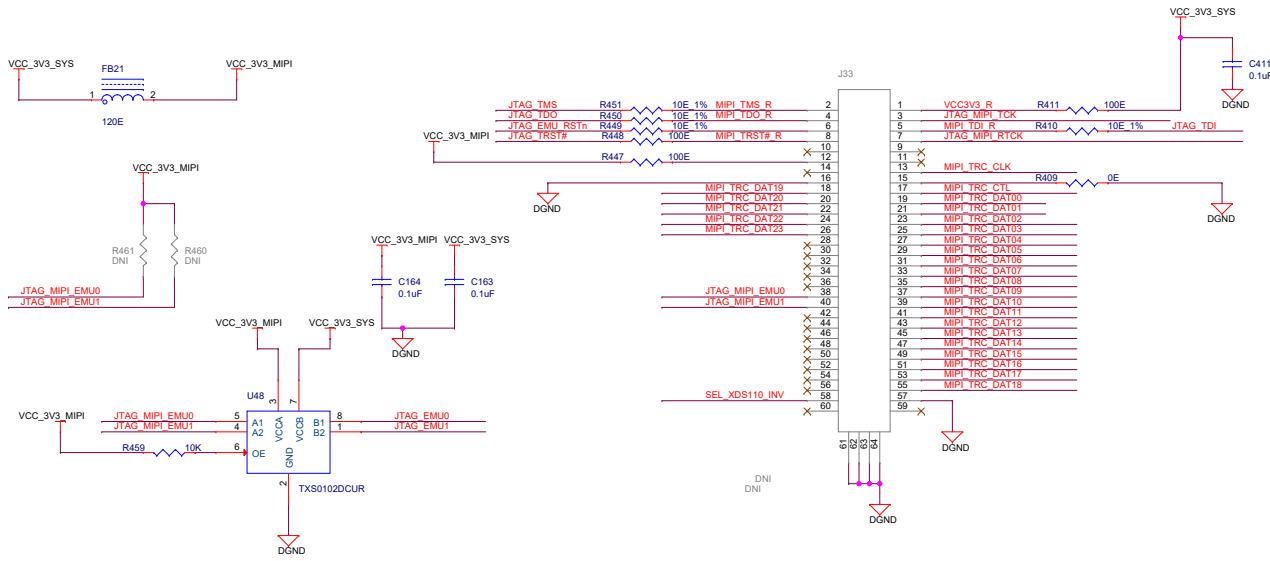
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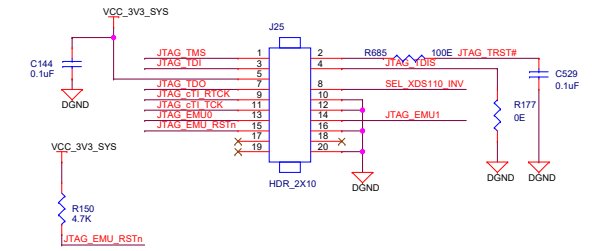
Title JTAG BUFFER

Size	Variant Name = PROC101A(001)TMD864PEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 23 of 40

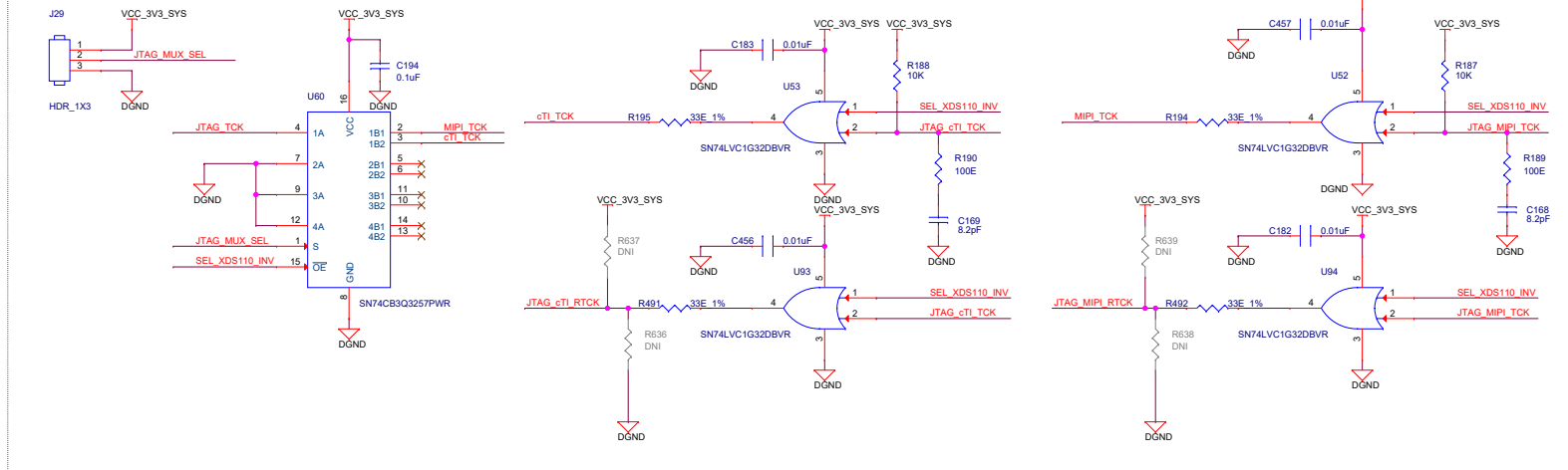
MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



Off Page Connections

From JTAG Buffer

23	SEL_XDS110_INV	SEL_XDS110_INV
23	JTAG_TDO	JTAG_TDO
23	JTAG_EMU0	JTAG_EMU0
23	JTAG_EMU1	JTAG_EMU1
23	JTAG_TDI	JTAG_TDI
23	JTAG_TCK	JTAG_TCK
23	JTAG_TMS	JTAG_TMS
23	JTAG_TRST#	JTAG_TRST#
35	JTAG_EMU_RSTn	JTAG_EMU_RSTn

From SoC GPMC

28	MIPI_TRC_DAT05	MIPI_TRC_DAT05
28	MIPI_TRC_DAT06	MIPI_TRC_DAT06
28	MIPI_TRC_DAT07	MIPI_TRC_DAT07
28	MIPI_TRC_DAT08	MIPI_TRC_DAT08
28	MIPI_TRC_DAT09	MIPI_TRC_DAT09
28	MIPI_TRC_DAT10	MIPI_TRC_DAT10
28	MIPI_TRC_DAT11	MIPI_TRC_DAT11
28	MIPI_TRC_DAT12	MIPI_TRC_DAT12
28	MIPI_TRC_DAT13	MIPI_TRC_DAT13
28	MIPI_TRC_DAT14	MIPI_TRC_DAT14
28	MIPI_TRC_DAT15	MIPI_TRC_DAT15
28	MIPI_TRC_DAT16	MIPI_TRC_DAT16
28	MIPI_TRC_DAT17	MIPI_TRC_DAT17
28	MIPI_TRC_DAT18	MIPI_TRC_DAT18
28	MIPI_TRC_DAT19	MIPI_TRC_DAT19
28	MIPI_TRC_DAT20	MIPI_TRC_DAT20
28	MIPI_TRC_DAT21	MIPI_TRC_DAT21
28	MIPI_TRC_DAT22	MIPI_TRC_DAT22
28	MIPI_TRC_DAT23	MIPI_TRC_DAT23
28	MIPI_TRC_DAT24	MIPI_TRC_DAT24

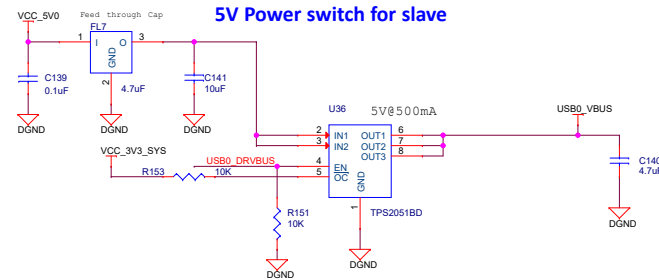
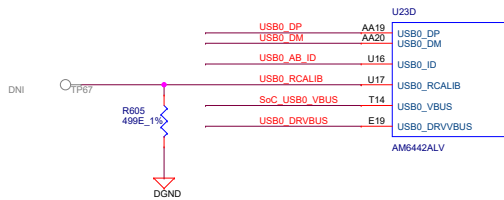
Designed for TI by Mistral Solutions Pvt Ltd



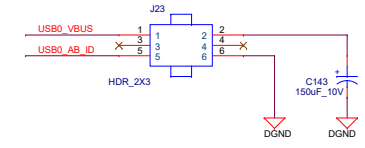
Title MIPI 60 PIN CONNECTOR

Size	Variant Name = PROC101A(001)TMD864PEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 24 of 40

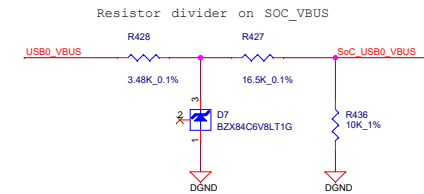
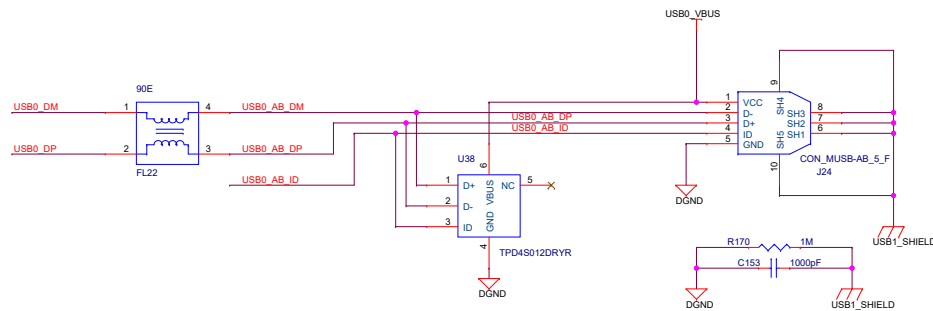
USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0_VBUS in host mode and to ground USB0_AB_ID pin, if a non standard cable is used



Micro USB 2.0 AB Connector



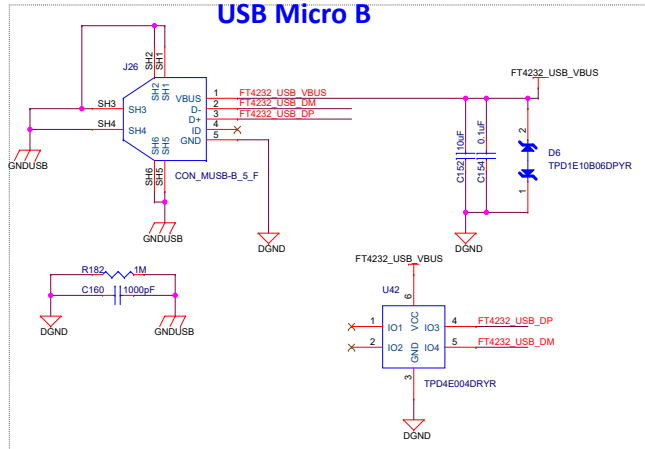
Designed for TI by Mistral Solutions Pvt Ltd



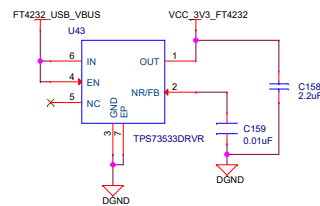
Title USB 2.0 INTERFACE

Size	Variant Name = PROC101A(001) TMD684GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 25 of 40

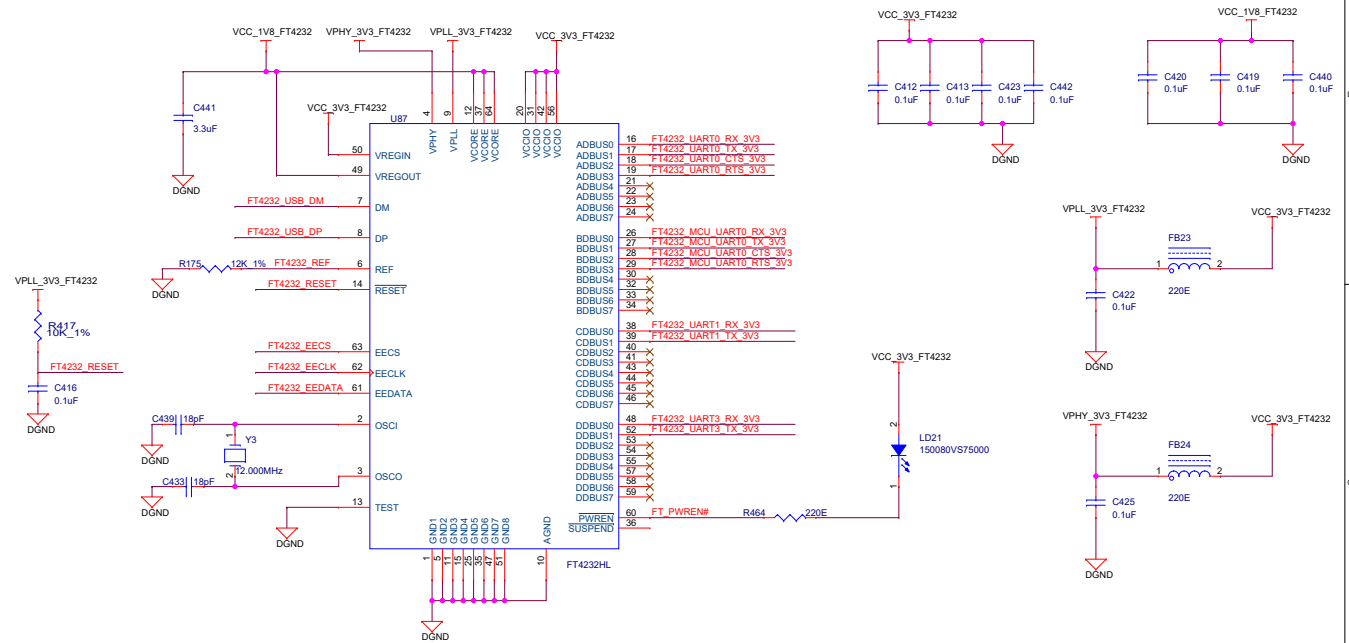
USB Micro B



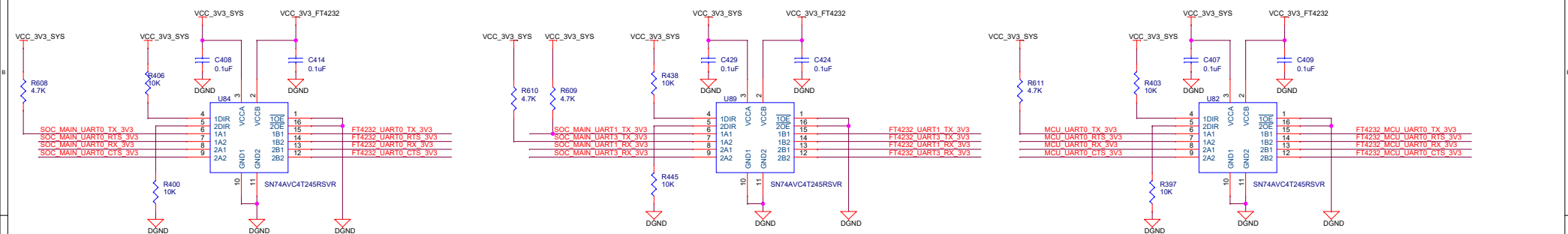
FT4232: 5V to 3.3V@500mA LDO



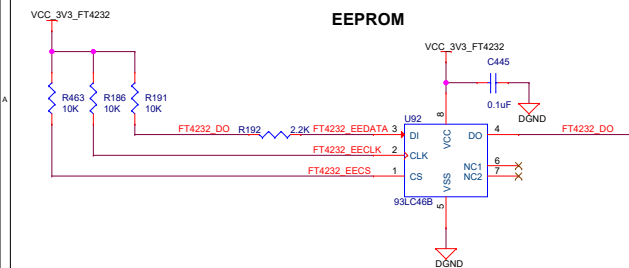
FT4232 UART



FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	SOC_MAIN_UART1_CTS_3V3	29

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Title FT4232 UART to USB BRIDGE

Size	Variant Name = PROC101A(001)TMD864PEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 26 of 40

PRG0 & PRG1

U23K

PRG0_MDIO0_MDC P3
PRG0_MDIO0_MDIO P2
PRG0_PRUI0GP00 U1
PRG0_PRUI0GP01 R4
PRG0_PRUI0GP02 U2
PRG0_PRUI0GP03 U3
PRG0_PRUI0GP04 A2
PRG0_PRUI0GP05 R3
PRG0_PRUI0GP06 F5
PRG0_PRUI0GP07 T1
PRG0_PRUI0GP08 T2
PRG0_PRUI0 GP07CPSW_RGMII_TX_CTL U6
PRG0_PRUI0 GP07CPSW_RGMII_RXC_A3
PRG0_PRUI0GP010 V3
PRG0_PRUI0GP013 A5
PRG0_PRUI0GP014 R6
PRG0_PRUI0GP015 U4
PRG0_PRUI0GP016 U1
PRG0_PRUI0GP017 U1
PRG0_PRUI0GP018 U1
PRG0_PRUI0GP019 W1
PRG0_PRUI0GP0 W2
PRG0_PRUI0GP1 V3
PRG0_PRUI0GP2 V4
PRG0_PRUI0GP3 W3
PRG0_PRUI0GP4 P4
PRG0_PRUI0GP5 R5
PRG0_PRUI0 GP07CPSW_RGMII_R0 W6
PRG0_PRUI0GP8 R1
PRG0_PRUI0 GP07CPSW_RGMII_R0Z V6
PRG0_PRUI0GP11 W4
PRG0_PRUI0GP12 U1
PRG0_PRUI0GP13 U6
PRG0_PRUI0GP14 U5
PRG0_PRUI0GP16 A4
PRG0_PRUI0 GP07CPSW_RGMII_RXC_A3
CPSW_RGMII_MDIO P5
CPSW_RGMII_MDC R2

U23L

PRG1_MDIO0_MDC YE
PRG1_MDIO0_MDIO A4B
PRG1_PRUI0_GP00 U7
PRG1_PRUI0_GP01 W8
PRG1_PRUI0_GP02 Y8
PRG1_PRUI0_GP03 Y8
PRG1_PRUI0_GP04 V13
PRG1_PRUI0_GP05 A4
PRG1_PRUI0_GP06 U13
PRG1_PRUI0_GP07 W13
PRG1_PRUI0_GP08 U14
PRG1_PRUI0_GP09 A4B
PRG1_PRUI0_GP10 U9
PRG1_PRUI0_GP11 W9
PRG1_PRUI0_GP12 W9
PRG1_PRUI0_GP13 W9
PRG1_PRUI0_GP14 U9
PRG1_PRUI0_GP15 U9
PRG1_PRUI0_GP16 U9
PRG1_PRUI0_GP17 V7
PRG1_PRUI0_GP18 W7
PRG1_PRUI0_GP19 W7
PRG1_RGMII_R0 W11
PRG1_RGMII_R0Z AX12
PRG1_RGMII_R03 Y12
PRG1_RGMII_RX_CTL W15
PRG1_ET12_LED_1000RX_ER AX13
PRG1_RGMII_RXC U11
PRG1_RGMII_TX_CTL V15
PRG1_ET12_LED_LINK U12
PRG1_RGMII_T0 V15
PRG1_RGMII_T0Z W14
PRG1_RGMII_T02 AX10
PRG1_RGMII_T03 V10
PRG1_RGMII_T0Z U10
PRG1_RGMII_TXC AX11
PRG1_RGMII_TXC U10
PRG1_RGMII_T03 V10
PRG1_RGMII_T0Z U10
PRG1_PRUI0GP10 W12

[illegible]

The diagram illustrates the pin connections for the STM32MP13. It shows four pin headers: J2A, J2B, J2C, and J2D. Each header has 20 pins. The connections are as follows:

- J2A:**
 - A1: VCC_5V0_HSE
 - A2: PRG0_MDI0Q_MDI0
 - A3: PRG0_MDI0Q_MDC
 - A4: PRG0_MDI0Q_MDC
 - A5: PRG0_MDI0Q_MDC
 - A6: PRG0_MDI0Q_MDC
 - A7: PRG0_MDI0Q_MDC
 - A8: PRG0_MDI0Q_MDC
 - A9: PRG0_MDI0Q_MDC
 - A10: PRG0_MDI0Q_MDC
 - A11: PRG0_MDI0Q_MDC
 - A12: PRG0_MDI0Q_MDC
 - A13: PRG0_MDI0Q_MDC
 - A14: PRG0_MDI0Q_MDC
 - A15: PRG0_MDI0Q_MDC
 - A16: PRG0_MDI0Q_MDC
 - A17: PRG0_MDI0Q_MDC
 - A18: PRG0_MDI0Q_MDC
 - A19: PRG0_MDI0Q_MDC
 - A20: PRG0_MDI0Q_MDC
- J2B:**
 - B1: VCC_1V8_HSE
 - B2: PRG0_MDI0Q_MDC
 - B3: PRG0_MDI0Q_MDC
 - B4: PRG0_MDI0Q_MDC
 - B5: PRG0_MDI0Q_MDC
 - B6: PRG0_MDI0Q_MDC
 - B7: PRG0_MDI0Q_MDC
 - B8: PRG0_MDI0Q_MDC
 - B9: PRG0_MDI0Q_MDC
 - B10: PRG0_MDI0Q_MDC
 - B11: PRG0_MDI0Q_MDC
 - B12: PRG0_MDI0Q_MDC
 - B13: PRG0_MDI0Q_MDC
 - B14: PRG0_MDI0Q_MDC
 - B15: PRG0_MDI0Q_MDC
 - B16: PRG0_MDI0Q_MDC
 - B17: PRG0_MDI0Q_MDC
 - B18: PRG0_MDI0Q_MDC
 - B19: PRG0_MDI0Q_MDC
 - B20: PRG0_MDI0Q_MDC
- J2C:**
 - C1: VCC_1V8_HSE
 - C2: PRG0_MDI0Q_MDC
 - C3: PRG0_MDI0Q_MDC
 - C4: PRG0_MDI0Q_MDC
 - C5: PRG0_MDI0Q_MDC
 - C6: PRG0_MDI0Q_MDC
 - C7: PRG0_MDI0Q_MDC
 - C8: PRG0_MDI0Q_MDC
 - C9: PRG0_MDI0Q_MDC
 - C10: PRG0_MDI0Q_MDC
 - C11: PRG0_MDI0Q_MDC
 - C12: PRG0_MDI0Q_MDC
 - C13: PRG0_MDI0Q_MDC
 - C14: PRG0_MDI0Q_MDC
 - C15: PRG0_MDI0Q_MDC
 - C16: PRG0_MDI0Q_MDC
 - C17: PRG0_MDI0Q_MDC
 - C18: PRG0_MDI0Q_MDC
 - C19: PRG0_MDI0Q_MDC
 - C20: PRG0_MDI0Q_MDC
- J2D:**
 - D1: VCC_1V8_HSE
 - D2: PRG0_MDI0Q_MDC
 - D3: PRG0_MDI0Q_MDC
 - D4: PRG0_MDI0Q_MDC
 - D5: PRG0_MDI0Q_MDC
 - D6: PRG0_MDI0Q_MDC
 - D7: PRG0_MDI0Q_MDC
 - D8: PRG0_MDI0Q_MDC
 - D9: PRG0_MDI0Q_MDC
 - D10: PRG0_MDI0Q_MDC
 - D11: PRG0_MDI0Q_MDC
 - D12: PRG0_MDI0Q_MDC
 - D13: PRG0_MDI0Q_MDC
 - D14: PRG0_MDI0Q_MDC
 - D15: PRG0_MDI0Q_MDC
 - D16: PRG0_MDI0Q_MDC
 - D17: PRG0_MDI0Q_MDC
 - D18: PRG0_MDI0Q_MDC
 - D19: PRG0_MDI0Q_MDC
 - D20: PRG0_MDI0Q_MDC

The diagram also shows the internal connections of the STM32MP13, including the SOC, PRG0, and PRG1 blocks, and the various peripheral blocks like the GPIOs, I2C, and SPI.

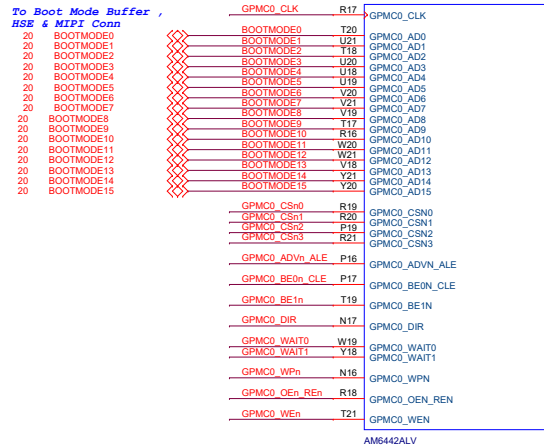
To Presence Detect Buffer	15	HSE_DETECT	↔	HSE_DETECT
From Processor GPMC	28	GPMC0_CSn1	↔	GPMC0_CSn1
	28	GPMC0_CSn2	↔	GPMC0_CSn2
	28	GPMC0_CSn3	↔	GPMC0_CSn3
	28	GPMC0_DIR	↔	GPMC0_DIR
From FSI mux	28	GPMC0_A08	↔	GPMC0_A08
	28	GPMC0_A09	↔	GPMC0_A09
	28	GPMC0_A10	↔	GPMC0_A10
	28	GPMC0_A11	↔	GPMC0_A11
	28	GPMC0_A14	↔	GPMC0_A14
	28	GPMC0_A15	↔	GPMC0_A15
	28	HSE_GPIO0_38	↔	HSE_GPIO0_38
From Processor GPMC resistor muxed with MIP1	28	GPMC0_A00	↔	GPMC0_A00
	28	GPMC0_A01	↔	GPMC0_A01
	28	GPMC0_A02	↔	GPMC0_A02
	28	GPMC0_A03	↔	GPMC0_A03
	28	GPMC0_A04	↔	GPMC0_A04
	28	GPMC0_A05	↔	GPMC0_A05
	28	GPMC0_A06	↔	GPMC0_A06
	28	GPMC0_A07	↔	GPMC0_A07
	28	GPMC0_A11	↔	GPMC0_A11
	28	GPMC0_A12	↔	GPMC0_A12
	28	GPMC0_A13	↔	GPMC0_A13
	28	HSE_GPIO0_31	↔	HSE_GPIO0_31
	28	HSE_GPIO0_32	↔	HSE_GPIO0_32
	28	HSE_GPIO0_33	↔	HSE_GPIO0_33
	28	HSE_GPIO0_34	↔	HSE_GPIO0_34
	28	HSE_GPIO0_35	↔	HSE_GPIO0_35
	28	HSE_GPIO0_36	↔	HSE_GPIO0_36
	28	HSE_GPIO0_37	↔	HSE_GPIO0_37
	28	HSE_GPIO0_38	↔	HSE_GPIO0_38
	28	HSE_GPIO0_39	↔	HSE_GPIO0_39
	28	HSE_GPIO0_40	↔	HSE_GPIO0_40
From Processor	34	MCU_PORZ	↔	MCU_PORZ
	34,35	MCU_RESET#	↔	MCU_RESET#
	34	MCU_RESETStA	↔	MCU_RESETStAtz
	29	HSE_MCAN0_RXUART4_TXD	↔	HSE_MCAN0_RXUART4_TXD
	29	HSE_MCAN0_TXUART4_RXD	↔	HSE_MCAN0_TXUART4_RXD
	29	HSE_MCAN1_RXi2C3_SCL	↔	HSE_MCAN1_RXi2C3_SCL
	29	HSE_MCAN1_TXi2C3_SCL	↔	HSE_MCAN1_TXi2C3_SCL
	29	SOC_SP1_CLK	↔	SOC_SP1_CLK
	29	SOC_SP1_M0S0	↔	SOC_SP1_M0S0
	29	SOC_SP1_M0S0	↔	SOC_SP1_M0S0
	29	SOC_SP1_M0S1	↔	SOC_SP1_M0S1
	29	SOC_SP1_C51	↔	SOC_SP1_C51
	15,29,33	Soc_I2C0_SDA	↔	Soc_I2C0_SDA
	15,29,33	Soc_I2C0_SCL	↔	Soc_I2C0_SCL
From clock Buffer	31	PRG0_HSE_ETH1_CLK	↔	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	↔	PRG0_HSE_ETH2_CLK
To and from ICSSG1 Ethernet PHY	17	PRG1_RGMII2_RD0	↔	PRG1_RGMII2_RD0
	17	PRG1_RGMII2_RD1	↔	PRG1_RGMII2_RD1
	17	PRG1_RGMII2_RD2	↔	PRG1_RGMII2_RD2
	17	PRG1_RGMII2_RD3	↔	PRG1_RGMII2_RD3
	17	PRG1_RGMII2_RXC	↔	PRG1_RGMII2_RXC
	17	PRG1_RGMII2_TX_CTL	↔	PRG1_RGMII2_TX_CTL
	17	PRG1_ETH2_LED_1000RX_ER	↔	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMII2_TD0	↔	PRG1_RGMII2_TD0
	17	PRG1_RGMII2_TD1	↔	PRG1_RGMII2_TD1
	17	PRG1_RGMII2_TD2	↔	PRG1_RGMII2_TD2
	17	PRG1_RGMII2_TD3	↔	PRG1_RGMII2_TD3
	17	PRG1_RGMII2_TYC	↔	PRG1_RGMII2_TYC
	17	PRG1_RGMII2_TX_CTL	↔	PRG1_RGMII2_TX_CTL
	17,18	PRG1_MDIO_MD0	↔	PRG1_MDIO_MD0
	17,18	PRG1_ETH3_LED_LINK	↔	PRG1_ETH3_LED_LINK
To and from ICSSG2 RGMII 1 Ethernet PHY	17	PRG1_ETH2_LED_LINK	↔	PRG1_ETH2_LED_LINK
	18	PRG1_RGMII1_RD0	↔	PRG1_RGMII1_RD0
	18	PRG1_RGMII1_RD1	↔	PRG1_RGMII1_RD1
	18	PRG1_RGMII1_RD2	↔	PRG1_RGMII1_RD2
	18	PRG1_RGMII1_RD3	↔	PRG1_RGMII1_RD3
	18	PRG1_RGMII1_RXC	↔	PRG1_RGMII1_RXC
	18	PRG1_RGMII1_TX_CTL	↔	PRG1_RGMII1_TX_CTL
	18	PRG1_ETH3_LED_1000RX_ER	↔	PRG1_ETH3_LED_1000RX_ER
	18	PRG1_RGMII1_TD0	↔	PRG1_RGMII1_TD0
	18	PRG1_RGMII1_TD1	↔	PRG1_RGMII1_TD1
	18	PRG1_RGMII1_TD2	↔	PRG1_RGMII1_TD2
	18	PRG1_RGMII1_TD3	↔	PRG1_RGMII1_TD3
	18	PRG1_RGMII1_TYC	↔	PRG1_RGMII1_TYC
	18	PRG1_RGMII1_TX_CTL	↔	PRG1_RGMII1_TX_CTL
From MUX To HSE	16	HSE_PRG0_PRUI_GP07	↔	HSE_PRG0_PRUI_GP07
	16	HSE_PRG0_PRUI_GP09	↔	HSE_PRG0_PRUI_GP09
	16	HSE_PRG0_PRUI_GP010	↔	HSE_PRG0_PRUI_GP010
	16	HSE		



Date:	Friday, March 26, 2021	Sheet	27	of	40
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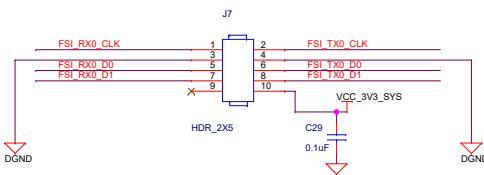
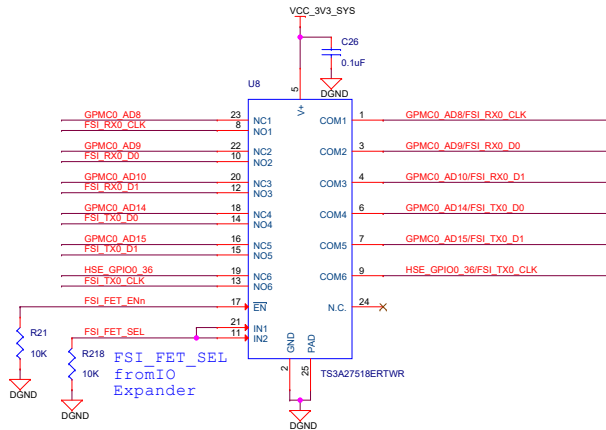
Date:	Friday, March 26, 2021	Sheet	27	of	40
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GPMC



GPMC TO FSI & HSE CONNECTOR

FSI CONNECTOR

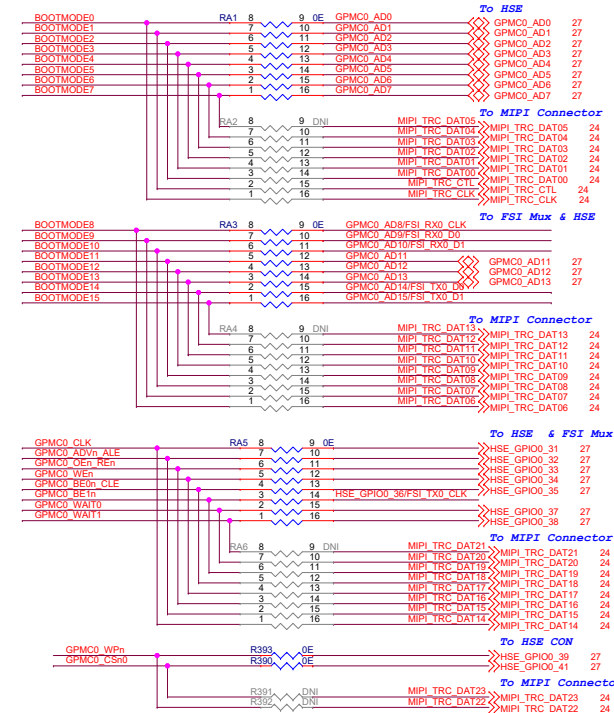


TS3A2751BRTWR Truth Table

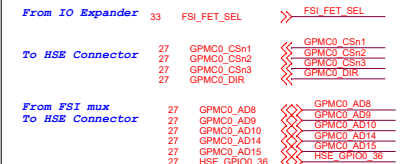
EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM1/2/3 & COM1/2/3 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391 & R392 Should be DNI'd.
-For TRACE RA2, RA4, RA6, R391 & R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



Off Page Connections



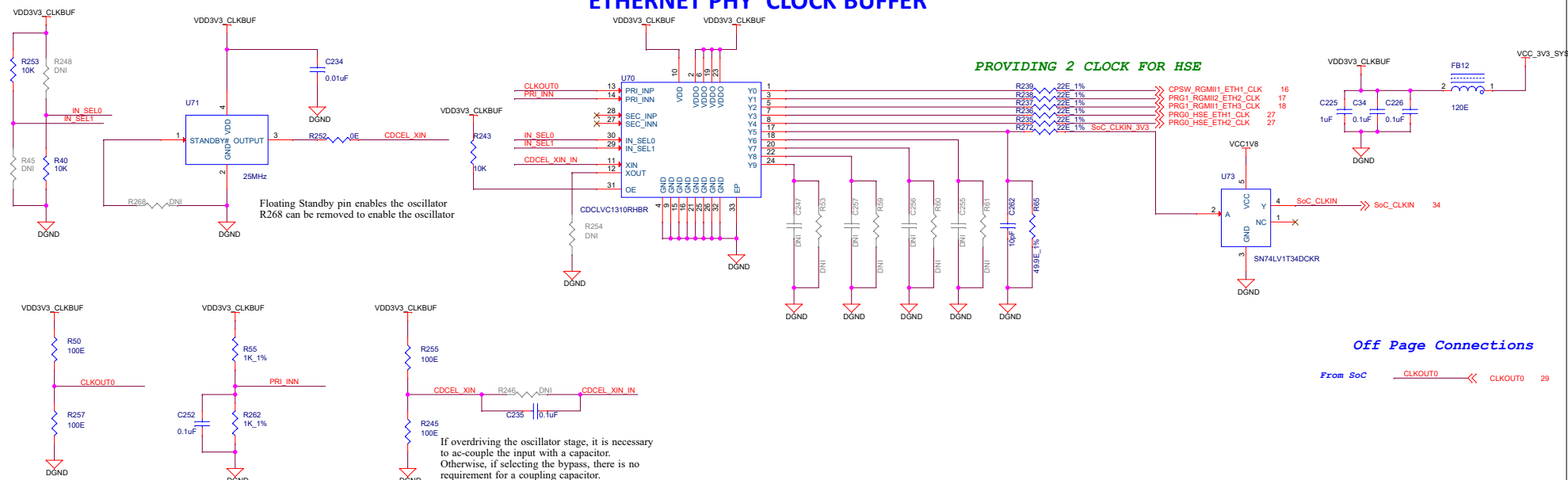
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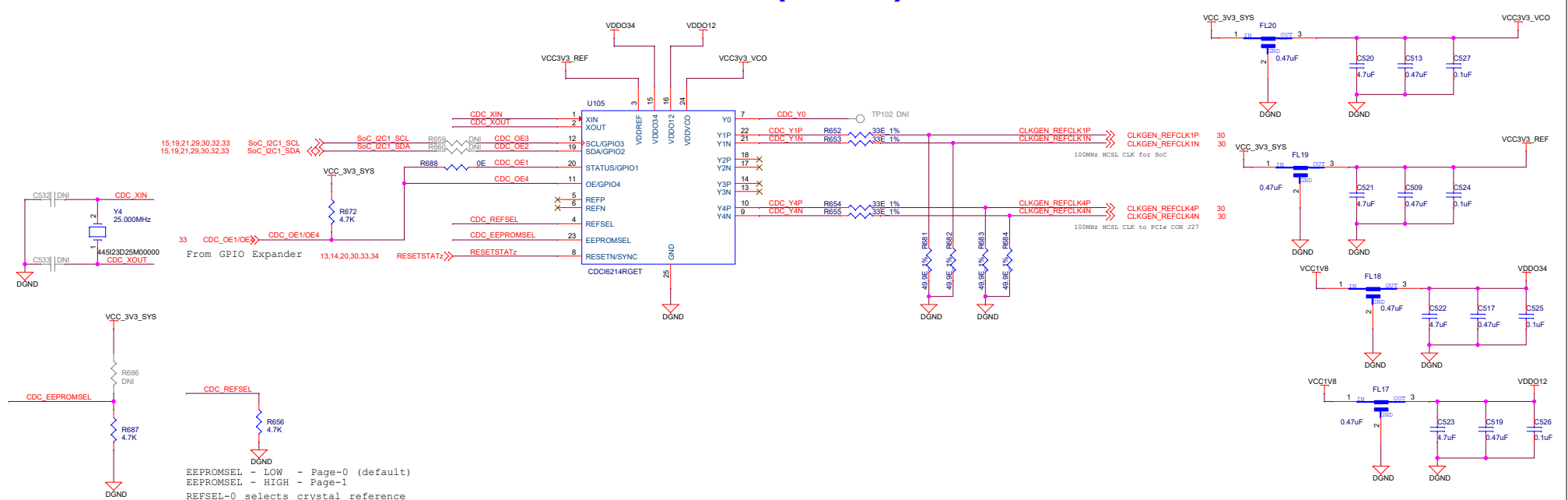
Title		GPMC	
Size	Variant Name = PROC101A(001)TMD864GPEVM	Rev	
C		E2	
Date:	Friday, March 26, 2021	Sheet	28 of 40

REFERENCE INPUT SELECTION

ETHERNET PHY CLOCK BUFFER



PCIe Clock HCSL (100MHz)



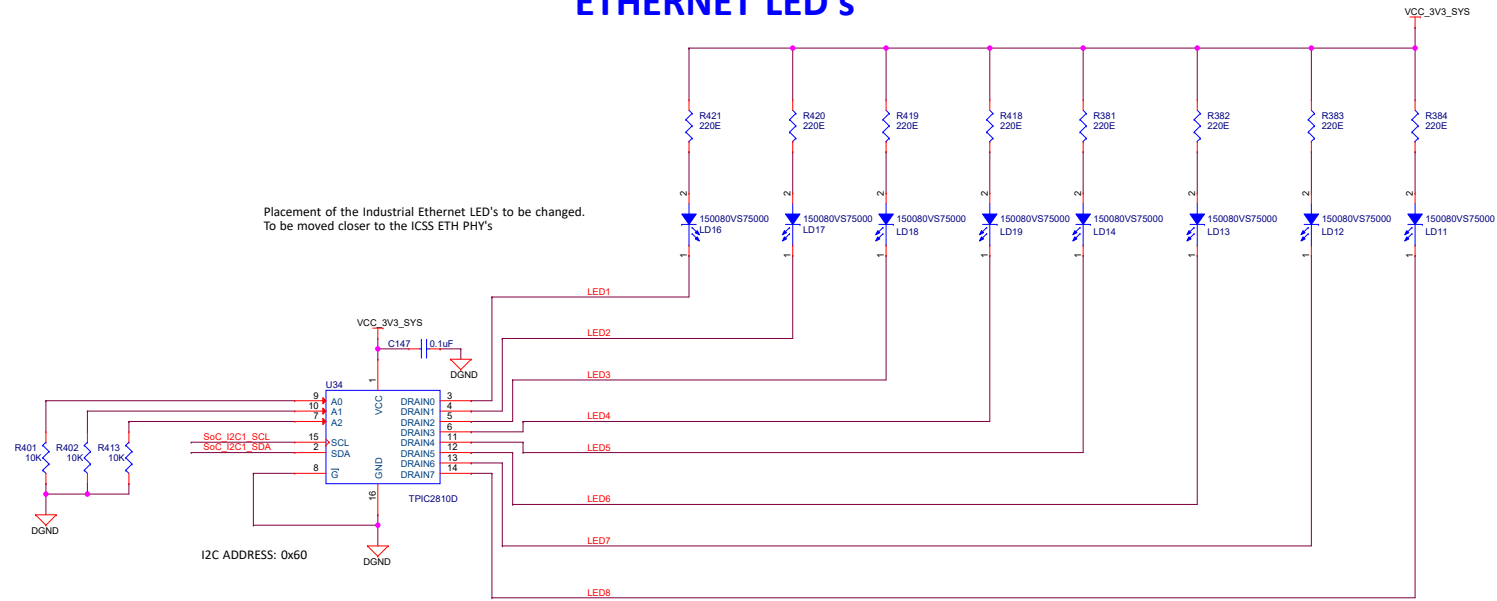
Designed for TI by Mistral Solutions Pvt Ltd



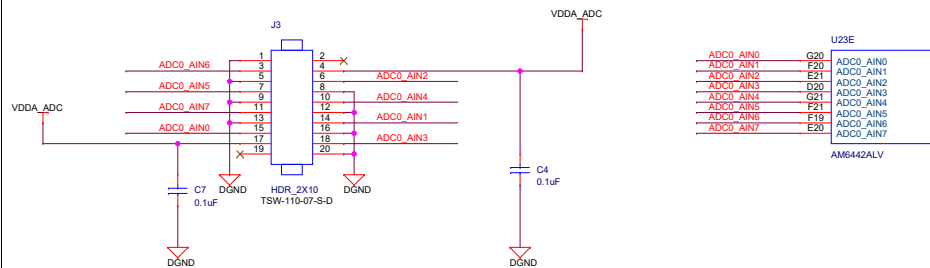
Title ETHERNET PHY & PCIe CLOCK GENERATOR

Size	Variant Name = PROC101A(001) TMD684GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 31 of 40

ETHERNET LED's



ADC CONNECTOR



Off Page Connections

SoC I2C1 SCL	15,19,21,29,30,31,33
SoC I2C1 SDA	15,19,21,29,30,31,33

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Title		ETHERNET LED's	
Size	Variant Name = PROC101A(001) TMD864GPEVM	Rev	E2
Date:	Friday, March 26, 2021	Sheet	32 of 40

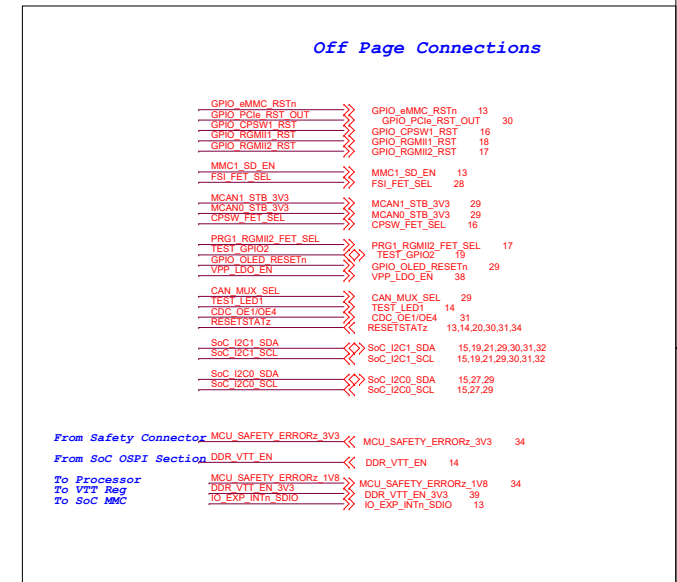
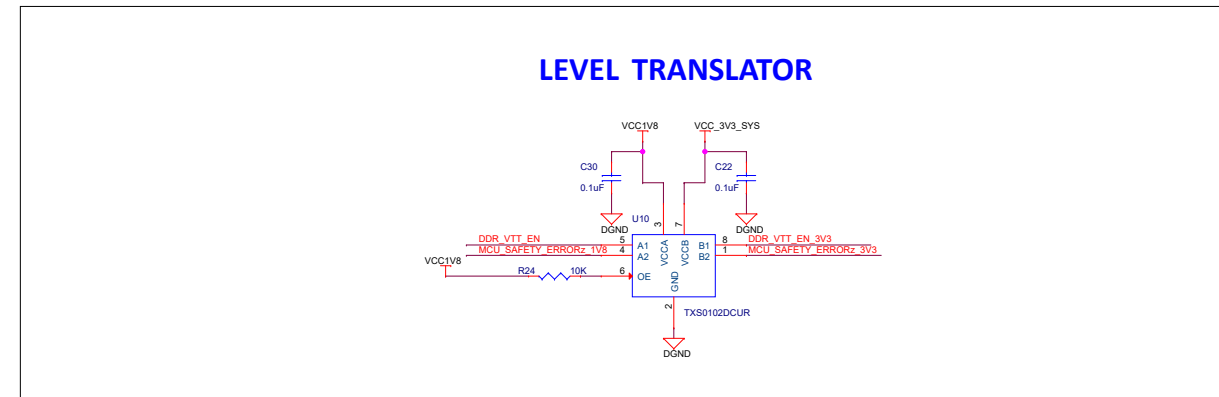
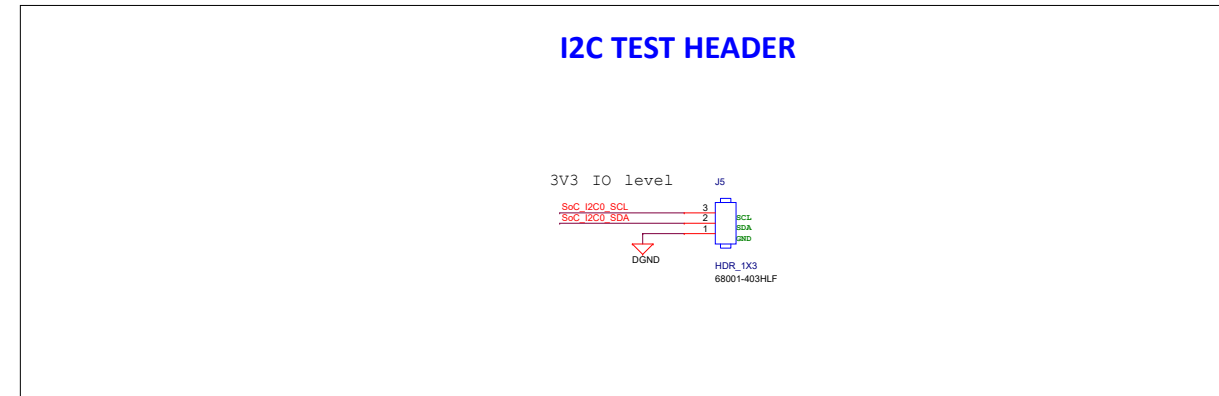
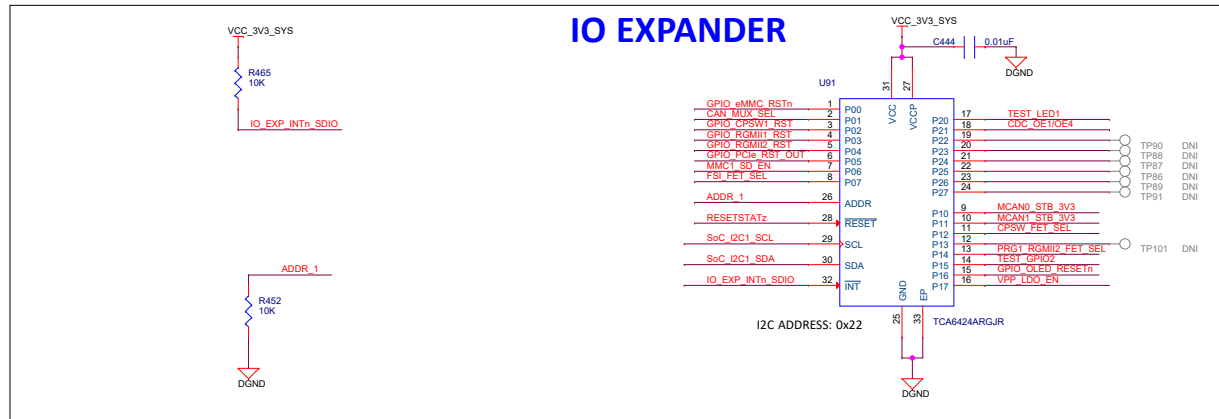


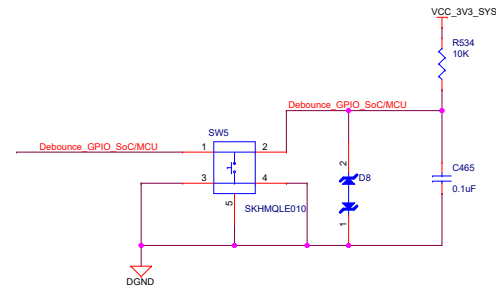
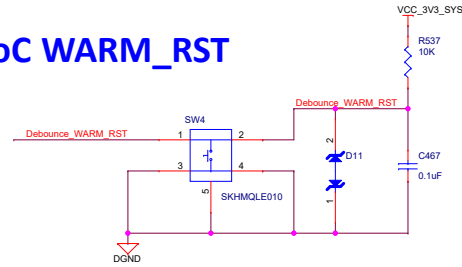
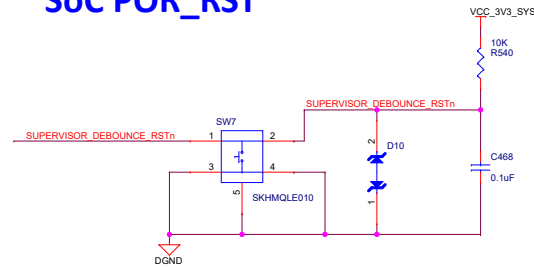
Figure 1: Schematic diagram of the processor power-up sequence. The diagram illustrates the internal circuitry and external components involved in the power-up process. Key components include the oscillator (Y1, 25.000MHz), the reset circuit (CONN MCU_RESETz), and the power supply pins (VCC_3V3_SYS). The diagram is divided into three main sections: the oscillator section, the reset section, and the power supply section.

- Oscillator Section:** The oscillator circuit (Y1) is connected to the MCU_OSC0_XI and MCU_OSC0_XO pins. It includes a 12pF capacitor (C133) and a 12pF capacitor (C134) connected to the oscillator pins. The oscillator is powered by a 25.000MHz crystal (ABM10W-25.000MHZ-8-K12-T3).
- Reset Section:** The reset circuit (CONN MCU_RESETz) is connected to the MCU_RESETz pin. It includes a 10K resistor (R6) connected to the reset pin and a 10K resistor (R7) connected to the reset pin.
- Power Supply Section:** The power supply pins (VCC_3V3_SYS) are connected to the power supply pins (R348, R344, R806). The power supply pins are connected to the power supply pins (R348, R344, R806) and the power supply pins (R348, R344, R806).

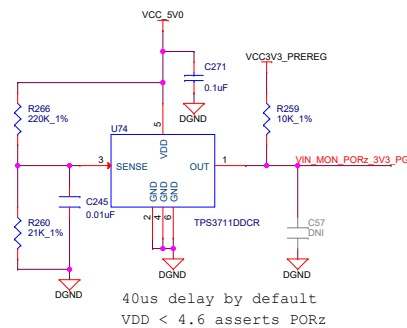
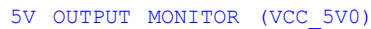
The diagram also shows the internal circuitry of the processor, including the oscillator (Y1), the reset circuit (CONN MCU_RESETz), and the power supply pins (VCC_3V3_SYS). The internal circuitry is connected to the external components (R137, R138, R139, R140, R6, R7, R348, R344, R806) and the external components (R137, R138, R139, R140, R6, R7, R348, R344, R806).

<i>To HSE Connector</i>	MCU_RESETSTAT2	MCU_RESET2	27	35
		MCU_RESETSTAT1	27	
<i>To level translator</i>	MCU_SAFETY_ERRORRZ_3V3	MCU_SAFETY_ERRORRZ_1V8		
<i>From Level Translator</i>	MCU_SAFETY_ERRORRZ_1V8	MCU_SAFETY_ERRORRZ_1V8		33
<i>To Boot Mode Selection</i>	PORZ_OUT	PORZ_OUT	13,16,17,18,20	
<i>From ICSSG Phyl1&2</i>	PRG1_RGMII_InTn	PRG1_RGMII_InTn	16,17,18	
<i>To User LED</i>	TEST_LED2	TEST_LED2	14	
<i>From Push button</i>	MCU_GPIO0_6	MCU_GPIO0_6	35	
<i>Switch</i>				
	SoC_CLKIN	SoC_CLKIN	31	
	MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26	
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26	
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26	
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26	

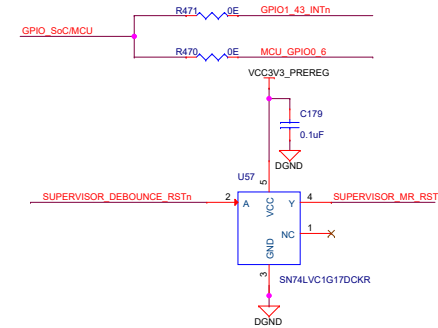
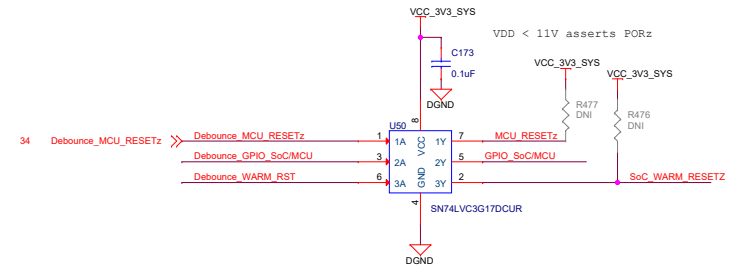
SoC WARM_RST



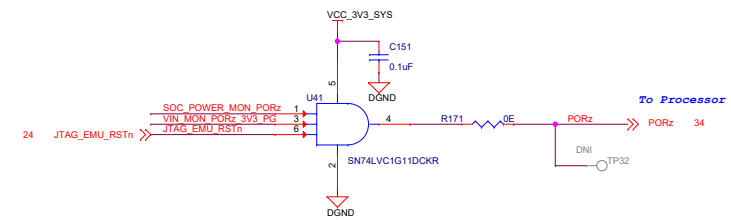
Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



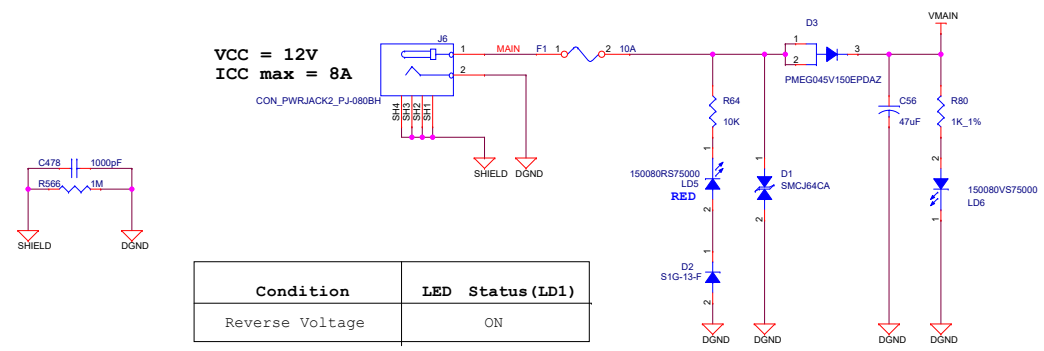
DEBOUNCE CIRCUIT



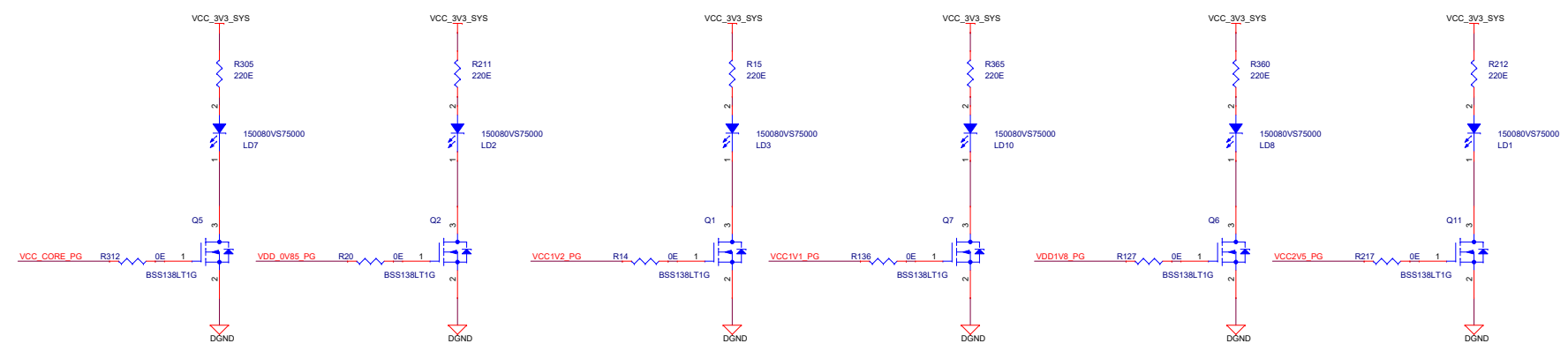
To Processor		
VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37.39
SoC_WARM_RESETz	SoC_WARM_RESETz	34
GPIO1_43_INtn	GPIO1_43_INtn	29
MCU_RESETz	MCU_RESETz	27.34
MCU_GPIO0_6	MCU_GPIO0_6	34



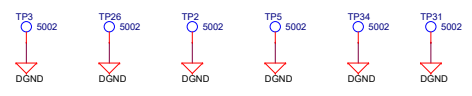
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

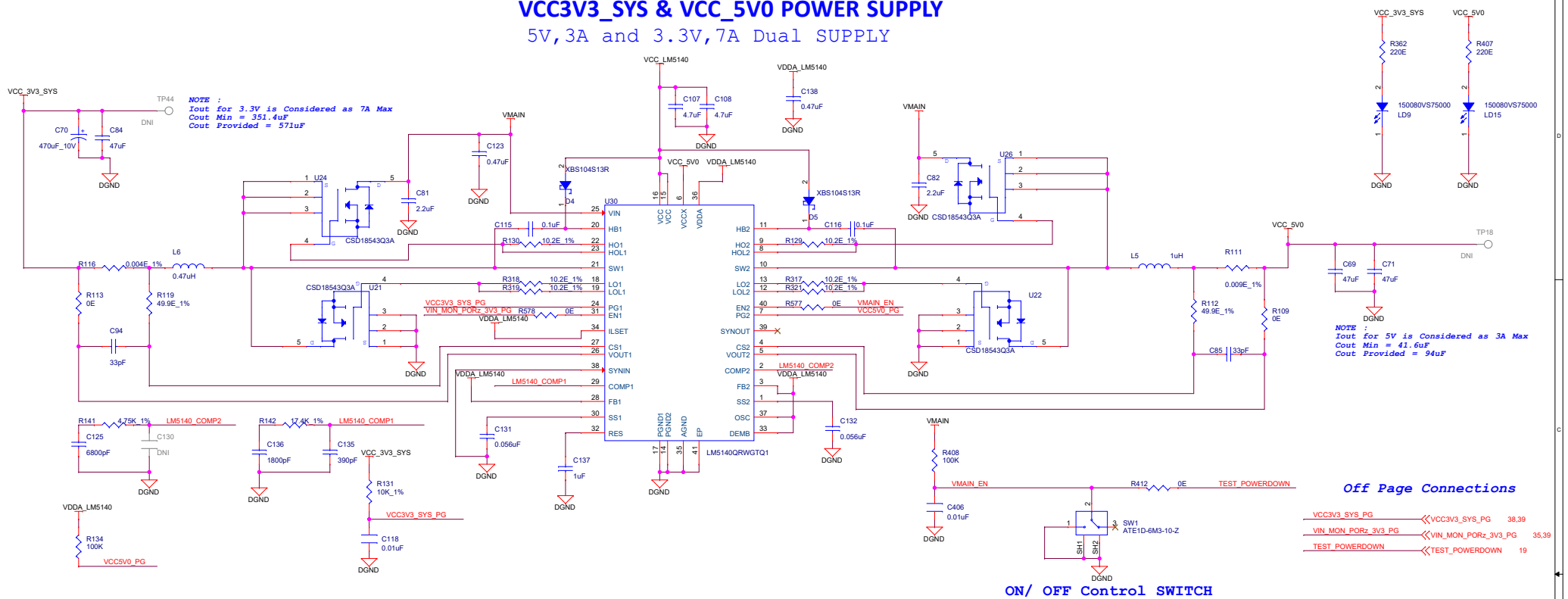
VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	38
VDD1V8_PG	VDD1V8_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

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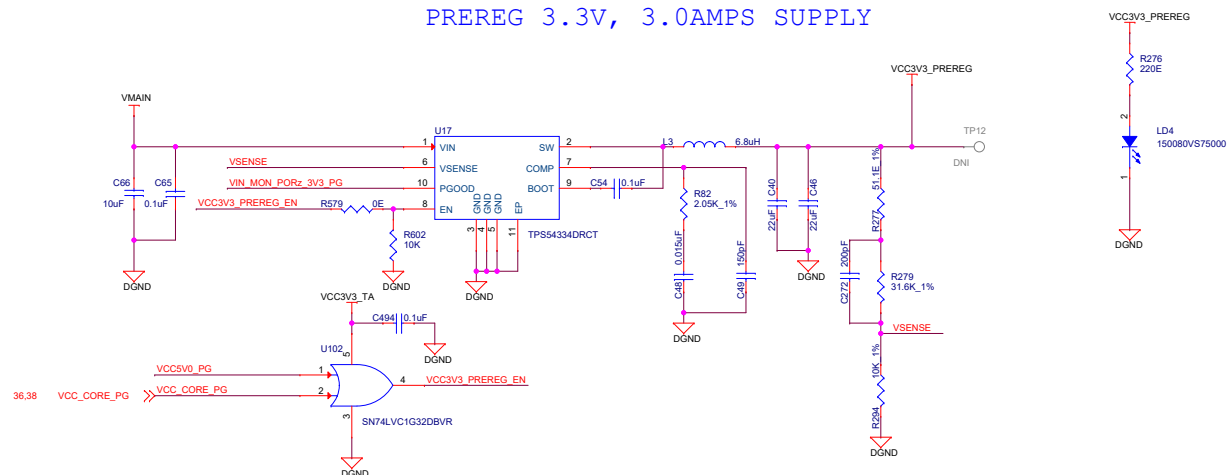


Title MAIN 12V POWERSUPPLY		
Size	Variant Name = PROC101A(001) TMD864GPEVM	
C	Rev E2	
Date:	Friday, March 26, 2021	Sheet 36 of 40

VCC3V3_SYS & VCC_5V0 POWER SUPPLY

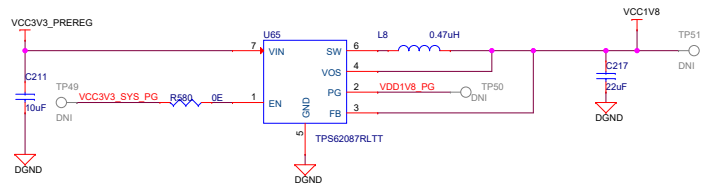


```
PREREG 3.3V, 3.0AMPS SUPPLY
```

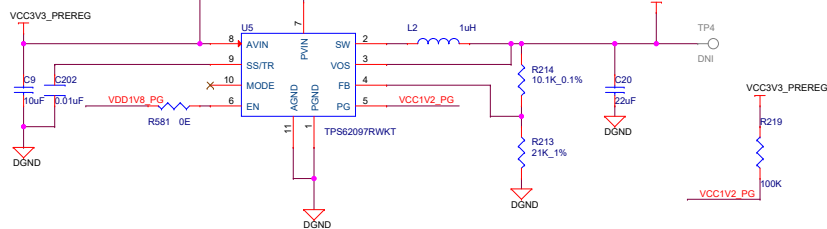


SoC POWER SUPPLY

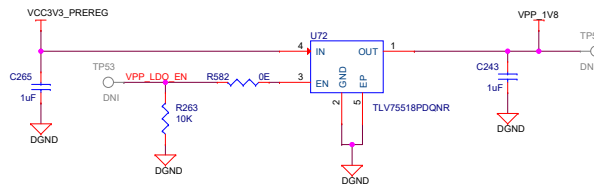
1.8V IO, 3.0AMPS SUPPLY



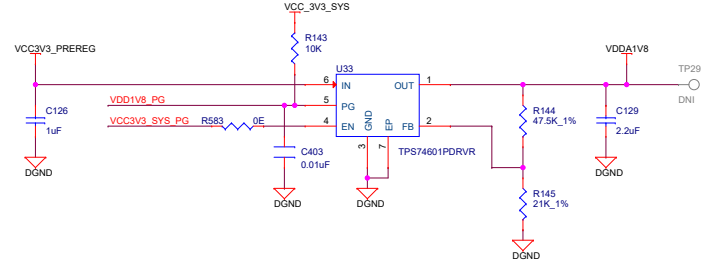
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



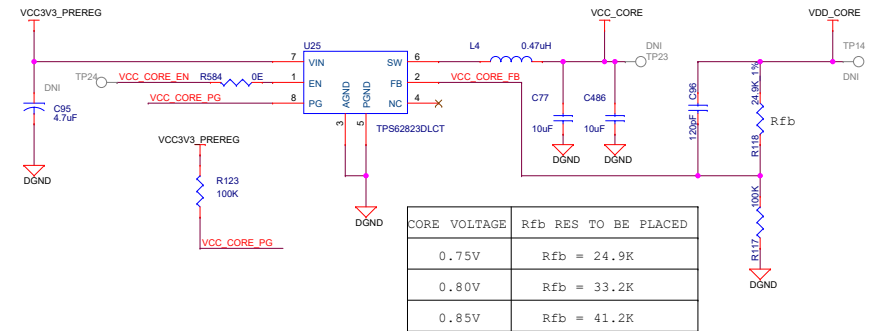
1.8V Analog , 1AMPS SUPPLY



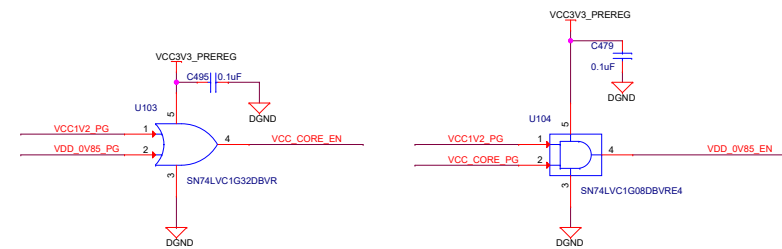
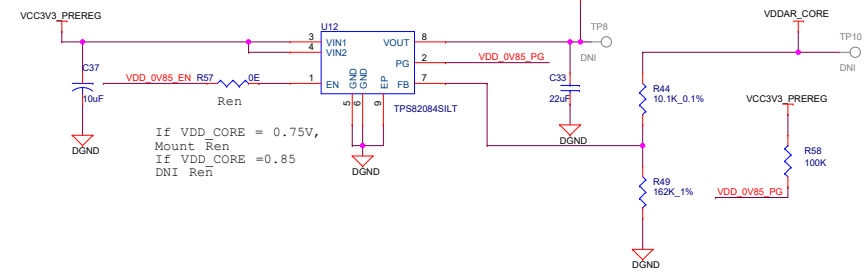
Off Page Connections

36.37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_OV85_PG	VDD_OV85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
33	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



0.85 V, 1.5AMPS SUPPLY



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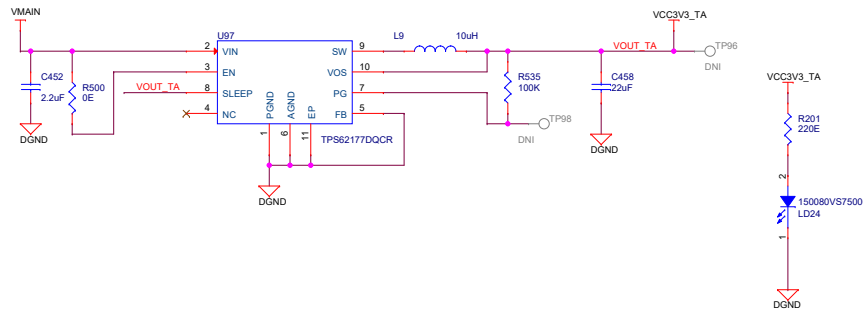


Title SoC POWER SUPPLY

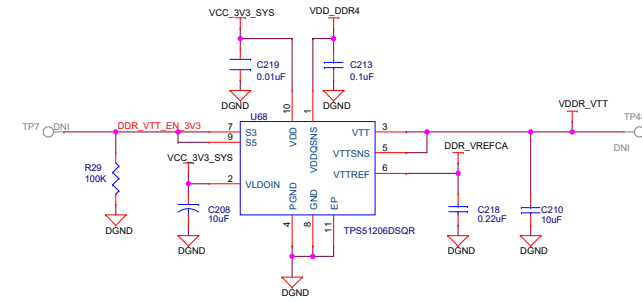
Size	Variant Name = PROC101A(001)TMD864PEVM	Rev
C		E2
Date:	Tuesday, March 30, 2021	Sheet 38 of 40

PERIPHERAL POWER SUPPLY

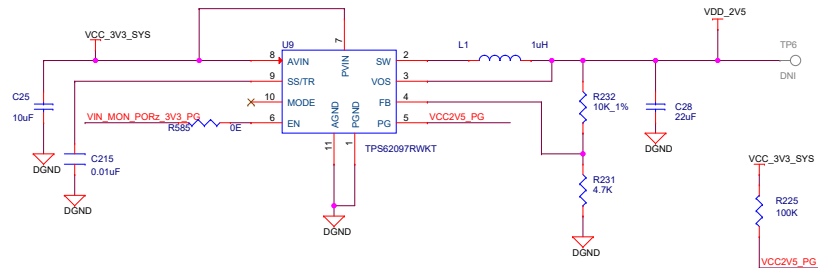
TEST AUTOMATION BOARD POWER



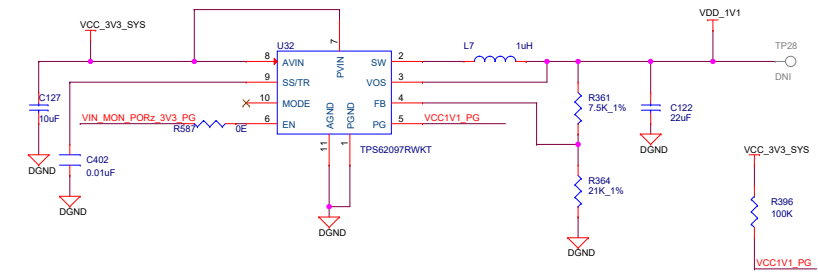
VTT SUPPLY FOR DDR4



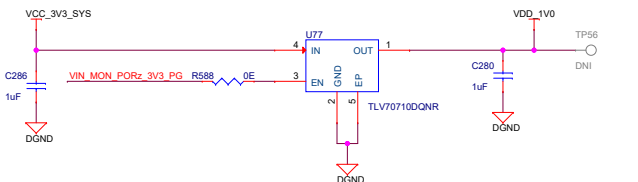
2.5V, 2.0AMPS SUPPLY



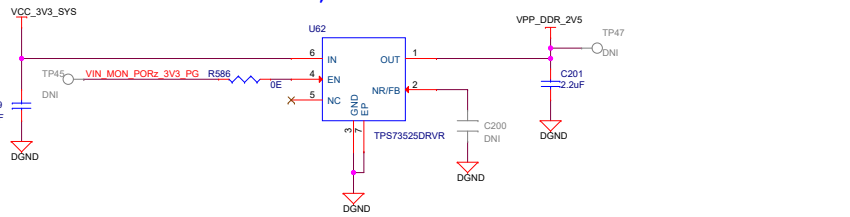
1.1V ETHERNET PHY POWER SUPPLY



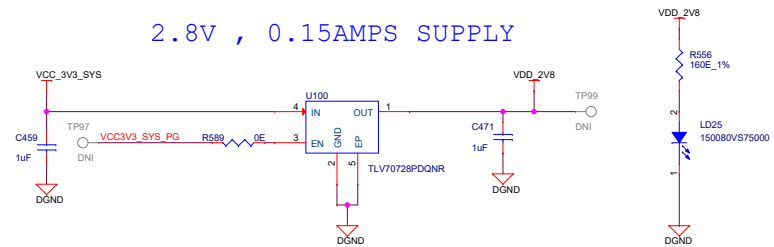
1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



2.8V , 0.15AMPS SUPPLY



Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

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Title PERIPHERAL POWER SUPPLY

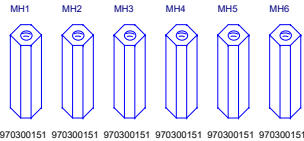
Size	Variant Name = PROC101A(001) TMD564PEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 39 of 40

HARDWARE SCHEMATICS

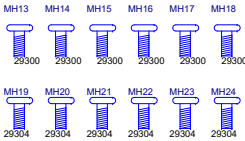
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

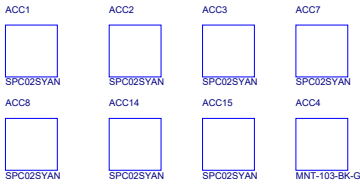
STANDOFFS



SCREWS



JUMPERS



WASHER'S



FIDUCIALS



RUBBER FEET



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

Board Serial No.



Assembly Revision

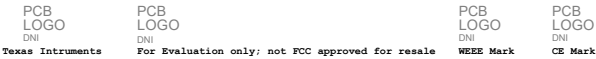


ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	
004	

LOGOS



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101A(001) TMDS64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 40 of 40